ACTIVITY REPORT

2021-2022

EUROPRACTICE

EUROPRACTICE

The access point to develop electronic components and systems

The EUROPRACTICE Service has received funding from the European Union through the H2020 framework program for research, technological development and demonstration under grant agreement N° 825121.

This funding is exclusively used to support European SMEs, universities and research laboratories.

FOREWORD

Dear customers, colleagues and friends,

We are leaving behind us another unusual year, and we hope that, wherever you are, life is slowly returning to normal. Despite the restrictions and consequences of the COVID-19 pandemic, we managed once again to keep uninterruptedly supporting you with access to microsystem technologies. This Activity Report summarises the results that we achieved together in the steady course of last year. Let us discuss them while looking forward to new horizons and challenges.

We could definitely feel the effect of the increased demand in the global semiconductor market. **In 2021, EUROPRACTICE customers submitted 985 designs.** We are very pleased to see that this is a ten-percent growth compared to the previous year, despite the supply shortages. Most of the designs (74%) were prototyped by European academia and industry.

The diversity of the fabricated designs reflects the constant growth of the EUROPRACTICE portfolio, which now includes technologies of 18 foundries. The use of advanced technologies has significantly increased. For instance, the number of designs in FDSOI technologies of STMicroelectronics and GLOBALFOUNDRIES has grown from 23 in 2020 to 84 last year. We can also see a quickly increasing number of FinFET prototypes manufactured at GLOBALFOUNDRIES and TSMC, with nodes ranging from 16 to 6 nm. Among More-than-Moore devices, we are glad to see an increase in the number of prototypes in GaN-IC: It rose from 2 in 2020 to 11 last year, indicating the growing popularity of this technology.

In 2021, most conferences and exhibitions still took place online. To facilitate interaction with our stakeholders, we tried different types of virtual events, such as a panel discussion at ESSCIRC-ESSDERC2021 and two online industry-cluster events co-organised with DSP Valley and Silicon Saxony respectively. We also continued to further increase our digital presence. For instance, the EUROPRACTICE LinkedIn has now more than 1900 followers. Next, we hosted three more very successful webinar series dedicated to MEMS technologies, flexible electronics and imec MPW services. Recordings of all our webinars are available on the YouTube channel of EUROPRACTICE. In addition, we restyled and restructured our websites to make the navigation more intuitive and the overall experience more user-friendly. Finally, our physical training courses were reconfigured and adapted to be presented online as live instructor-led training, including hands-on practical sessions using remotely accessible design tool environments.

In 2022, EUROPRACTICE will continue growing and providing you with high-quality services. Over the past year, our offer has been significantly extended. For instance, the Glass Microfluidics process of IMT has been included and can be combined with a newly added Noble Metal Module from X-FAB. Further, the Photonics offer has been enlarged with Glass Photonics of Teem Photonics, and Si-Photonics technologies of GLOBALFOUNDRIES and CORNERSTONE. MEMS portfolio has been reinforced by new PiezoMEMS processes from Tyndall National Institute. In the beginning of 2022, the Silicon-Carbide technology from Fraunhofer IISB has been added to the CMOS portfolio. Finally, the System Integration part includes now Fan-Out Wafer-Level Packaging (FOWLP) provided by Fraunhofer IZM. Together with enlarging our technology offer, we will keep organising webinars and delivering training courses that we hope will soon become face-to-face events.

We thank the European Commission (DG Connect) for their support. In 2022, we will work to secure an extension of our program within HORIZON Europe. The EC funding ensures that EUROPRACTICE services can continue providing the European academia and SMEs easy and affordable access to state-of-the-art design tools and IC technologies.

Finally, we thank all of you – our academic and industrial customers, our technology and design tool suppliers – for supporting our services, and we wish you all a productive and successful 2022.

Looking forward to supporting your innovative projects and creating more success stories together,

Romano Hoofman (EUROPRACTICE General Manager)
On behalf of the entire EUROPRACTICE team at imec, UKRI-STFC, Fraunhofer IIS, CMP and Tyndall

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EUROPRACTICE SERVICES

THE ACCESS POINT FOR ELECTRONIC COMPONENTS AND SYSTEMS

EUROPRACTICE offers a platform to develop electronic circuits and smart integrated systems. For more than 25 years, we have provided the European academia and industry with affordable access to a wide range of CAD tools, training courses and state-of-the-art fabrication technologies. We support customers in all critical steps on the way from prototype design to volume production.

OUR OFFER

A true one-stop shop, EUROPRACTICE provides all range of services needed to design and fabricate electronic devices and systems, complemented by extensive customer support:

- Affordable access to industry-standard and state-of-the-art design (CAD) tools, especially for European academia and start-ups
- Prototyping in multiple technologies, such as ASICs, Photonics, MEMS and Microfluidics, via Multi-Project-Wafer (MPW) runs
- Smart system integration and advanced packaging
- Route to volume production, including test and characterization services
- Training courses and webinars in design flows and on various technologies

OUR STORY

EUROPRACTICE was launched by the European Commission in 1995 succeeding its forerunner EUROCHIP (1989-1995). The service aimed to enhance European industrial competitiveness in the global marketplace by opening easy access to design tools and IC prototyping.

Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by supporting more than 600 European universities and research institutes, and over 300 SMEs.

Our current consortium members are imec (Belgium), UKRI-STFC (UK), Fraunhofer IIS (Germany), CMP (France) and Tyndall National Institute (Ireland). The two latter partners have joined the EUROPRACTICE consortium and reinforced it with their expertise at the start of the NEXTS project.

NEXTS is a three-year H2020 project funded by European Commission, addressing the call topic ICT-07-2018: Electronic Smart Systems (ESS). NEXTS stands for "Next EUROPRACTICE eXtended Technologies and Services" as it continues and expands a well-established EUROPRACTICE service portfolio.

In NEXTS, we extend our support to the European SMEs and start-ups, in particularly those originating from universities and research labs. In addition, we encourage customers to adopt Smart System Integration to discover new technologies that enable new application possibilities.

EUROPRACTICE BUSINESS MODEL

The EUROPRACTICE business model is based on a coordinated brokerage service for industrial companies and academic institutions who look for affordable and easy access to technologies in the domain of electronic smart systems. The service builds on the many years' experience of five consortium partners: imec, UKRI-STFC, Fraunhofer IIS, CMP and Tyndall.

EUROPRACTICE offers customers technology access through a vast network of suppliers that includes design-tool and IP-library vendors, foundries, assembly and test houses – who all provide state-of-the-art industry-grade technologies.

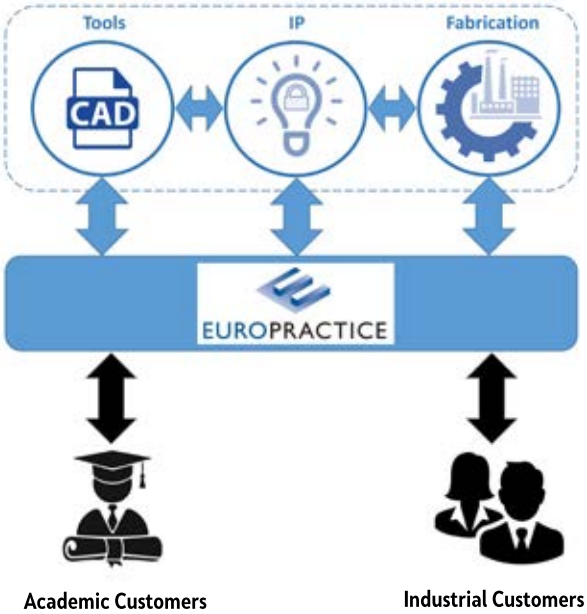

Fig. 1: Schematic representation of the entire EUROPRACTICE ecosystem, depicting a central role of the EUROPRACTICE service as prime interface between the technology suppliers (on top) and the customers (at the bottom).

The overall concept is that EUROPRACTICE acts as the prime interface between the customers and the technology providers. Such a prime interface (or one-stop function) has advantages for both the supply and demand side of the value chain. It is schematically represented in Figure 1, where the supply side is depicted on top, the demand side at the bottom and EUROPRACTICE in the centre.

The supply side corresponds with the current service portfolio, where design tools are provided by design-tool vendors, IP by dedicated library vendors and fabrication services by various foundries. In addition, the portfolio is extended with emerging technologies typically offered by leading research institutes, and technologies brokered by other service providers (such as CMC in Canada for Silicon Photonics by AMF).

Although EUROPRACTICE represents a large customer base, it is considered as one user by its suppliers. Design tool vendors, IP-vendors and foundries need to deal only with EUROPRACTICE to have their products and technologies promoted and securely distributed all over Europe. Thanks to this, EUROPRACTICE has been able to negotiate technology access on very favourable terms for its customers. This would not be possible when operating on a national level with only few users. Since the service functions on a pan-European level, the know-how and experience has only to be built up once.

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AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

EUROPRACTICE has negotiated lower prices with the major design tool vendors world-wide, as well as with IP and programmable device vendors. Consequently, European academic institutions can access EUROPRACTICE licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics etc.) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the EUROPRACTICE service provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

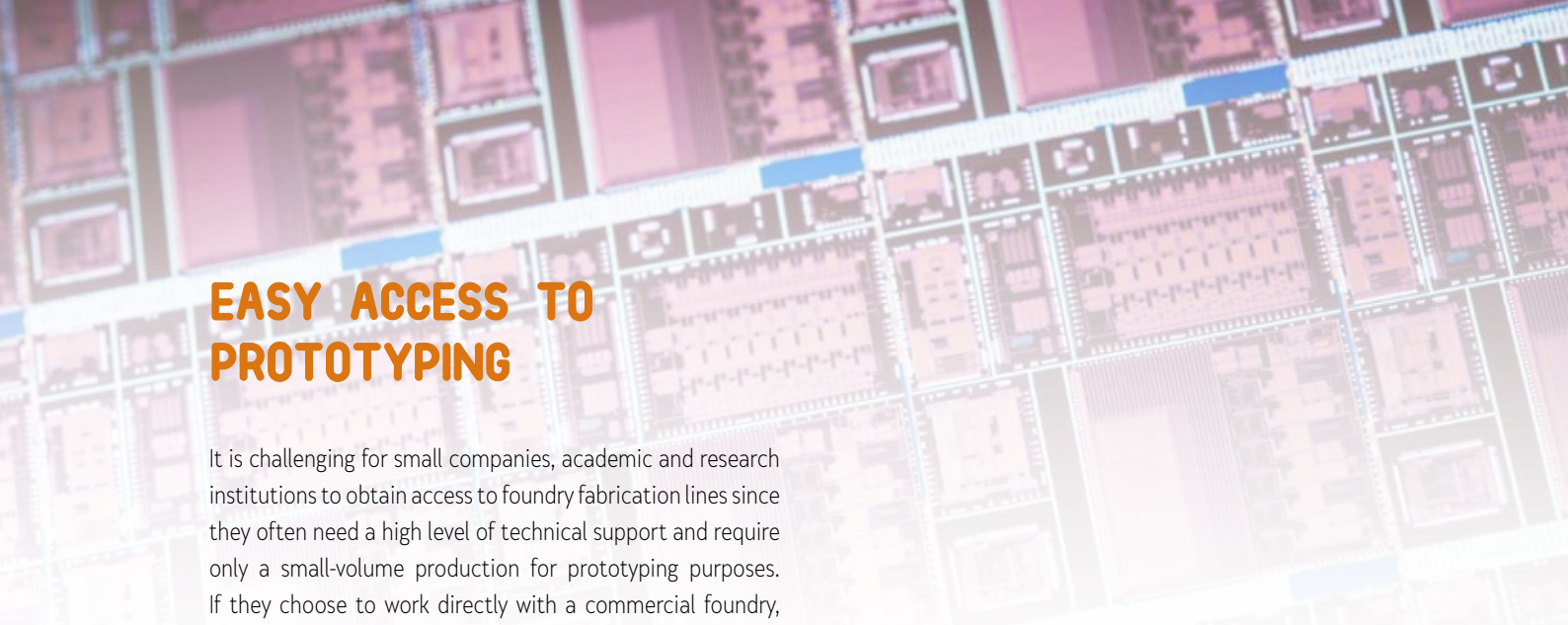
The current EUROPRACTICE network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows our customers to participate in EC-funded projects, ranging from IP block and component design to the design of complete systems.

arm · HDL Works · SIEMENS · cadence · imperas · softMEMS · CLIO SOFT · intel · SYNOPSYS · COVENTOR · IntelliSense · XILINX · DESIGN WORKSHOP TECHNOLOGIES · LUCEDA PHOTONICS · XJTAG

DESIGN TOOLS FOR SMEs

European SMEs can access certain design tools at low cost via EUROPRACTICE in order to produce a proof-of-concept IC to demonstrate their IP/product. The resultant IP can then be fully commercialized for an additional agreed fee. The SME gains access to an industry-standard full IC design flow, suitable for all IC technologies.

EUROPRACTICE works flexibly with academic institutes and SMEs to facilitate effective innovation. For instance, we have mechanisms in place if an academic institute has developed a design using EUROPRACTICE tools and subsequently wishes to exploit this design commercially, either via a spin-out or by transferring the IP to an existing SME.



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EASY ACCESS TO PROTOTYPING

It is challenging for small companies, academic and research institutions to obtain access to foundry fabrication lines since they often need a high level of technical support and require only a small-volume production for prototyping purposes. If they choose to work directly with a commercial foundry, the manufacturing costs will be very high.

This is when EUROPRACTICE comes into play. We help significantly reduce fabrication costs by opening access to Multi-Project-Wafer (MPW) runs and Multi-Level-Mask (MLM) services for prototyping and volume production respectively.

In addition, EUROPRACTICE offers a wide choice of technologies of world-leading foundries together with technical support and training.

TECHNOLOGY PORTFOLIO

In the beginning of 2021, the EUROPRACTICE portfolio included a broad range of technologies, such as ASIC processes ranging from 0.5µm to 12nm, MEMS, Si-Photonics and SiN-Photonics. The ASIC processes contained digital logic, RF, mixed-signal and high-voltage solutions.

Over the past year, this offer has been significantly extended. For instance, the Glass Microfluidics process of IMT has been included and can be combined with a newly added Noble Metal Module from X-FAB. Further, the Photonics offer has been enlarged with Glass Photonics of Teem Photonics, Si-Photonics 45nm SPCLO of GLOBALFOUNDRIES, SiN-Photonics and Suspended-Si technologies of CORNERSTONE. MEMS portfolio has been reinforced by new PiezoMEMS processes from Tyndall National Institute. In the beginning of 2022, the Silicon-Carbide High Temperature technology from Fraunhofer IISB has been added to the CMOS portfolio. Finally, the System Integration part includes now Fan-Out Wafer-Level Packaging (FOWLP) provided by Fraunhofer IZM.

Traditionally, EUROPRACTICE keeps focusing on technologies from European-based companies as 14 of the 18 foundries have manufacturing facilities in Europe.

MULTI PROJECT WAFER AND MINI@SIC RUNS

By combining several designs from different customers onto the same mask set of a prototype run, known as Multi-Project-Wafer (MPW) run, the high cost of the mask set and the fabrication process is shared among the participating customers.

Fabrication of prototypes can therefore be as low as 5% to 10% of the cost of a wafer run for only one dedicated customer. A limited number of IC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time". To achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

Since most of the designs fabricated for educational purposes are much smaller than the minimum block size on regular MPW runs, the concept of **mini@sic** was introduced in 2003. This solution allows to further lower prototype fabrication costs compared to standard MPW runs. The mini@sic principle is based on the following methodology: Several times per year, a foundry standard MPW block is bought and resold in smaller and cheaper sub-blocks or mini@sics. This program has been extended over the years and currently includes selected technologies from GLOBALFOUNDRIES, IHP, TSMC, UMC and X-FAB.

Recently, EUROPRACTICE has introduced a new ultra-flexible pricing solution for mini@sics in the most popular TSMC technologies. The minimum areas for customers have been significantly reduced (for instance, down to 1mm^2 for TSMC 28nm and 65nm) and their X and Y dimensions have become free to choose.

TECHNOLOGY PORTFOLIO 2022

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ams

- ams 0.35µm CMOS C35B4C3
- ams 0.35µm CMOS C35OPTO + BARC Diode option
- ams 0.35µm HV CMOS H35B4D3
- ams 0.35µm SiGe-BiCMOS S35
- WLSCP for ams C35B4C3

em microelectronic

- EM Microelectronic 0.18µm EMALPC18 logic

GlobalFoundries

- GF SiGe 8XP
- GF 130nm BCDlite-Gen2
- GF 55nm LPe-RF
- GF 45nm SPCLO Si-Photonics
- GF 45RFSOI
- GF 28nm SLPe
- GF 22nm FDSOI
- GF 12nm LP+

ihp

- IHP SGB25V 0.25µm SiGe:C
- IHP SG25H3 0.25µm SiGe:C
- IHP SG25H5_EPIC (BiCMOS + Photonics)
- IHP SG25 PIC (Photonics)
- IHP SG13S 0.13µm SiGe:C
- IHP SG13C 0.13µm SiGe:C
- IHP SG13G2 0.13µm SiGe:C
- IHP SG13G2Cu FEOL + Cu BEOL option
- IHP SG13SCu FEOL + Cu BEOL option
- IHP BEOL SG13
- IHP SG13S + MEMRES Module

ST

- ST 28nm CMOS28FDSOI
- ST 55nm BiCMOS055
- ST 65nm CMOS065
- ST 130nm BiCMOS9MW
- ST 130nm HCMOS9GP
- ST 130nm HCMOS9A
- ST 0.16µm BCD8sP
- ST 0.16µm BCD8s-SOI

tsmc

- TSMC 0.18µm CMOS Log/MS/RF (G)*
- TSMC 0.18µm CMOS HV BCD Gen II*
- TSMC 0.13µm BCD+ (12")
- TSMC 0.13µm CMOS Log/MS/RF (G, LP)
- TSMC 90nm CMOS Log/MS/RF (G ,LP)
- TSMC 65nm CMOS Log/MS/RF (G, LP)
- TSMC 40nm CMOS Log/MS/RF (G, LP)
- TSMC 28nm CMOS Log/RF HPC/HPC+
- TSMC 16nm CMOS Log/RF FinFET Compact

UMC

- UMC L180 Logic GII, MM/RF
- UMC L130 Log/MM/RF
- UMC L110AE Log/MM/RF
- UMC L55N Log/MM/RF (SP)
- UMC L65N Log/MM/RF (LL)
- UMC 40N Log/MM – LP
- UMC 28N Log/MM – HPC

xfab

- X-FAB XH035 0.35µm HV
- X-FAB XH035 Noble Metal
- X-FAB XH018 0.18µm HV NVM E-Flash
- X-FAB XT018 0.18µm HV SOI
- X-FAB XS018 0.18µm OPTO
- X-FAB XP018 0.18 µm NVM
- X-FAB XR013 0.13µm RF SOI
- X-FAB XMB10 MEMS

amf

- AMF Si-Photonics

leti

- CEA-leti Si-Photonics Si-220
- CEA-leti Si-Photonics Si-310
- CEA-Leti SiN-Photonics Si_3N_4-800
- CEA-Leti MAD200 130nm NVM

CORNERSTONE

- CORNERSTONE Si-Photonics 220 passives/actives
- CORNERSTONE Si-Photonics 340 passives
- CORNERSTONE Si-Photonics 500 passives
- CORNERSTONE SiN-Photonics
- CORNERSTONE Suspended-Si

Fraunhofer

- Fan-Out Wafer-Level Packaging
- 4H-SiC CMOS High Temperature Technology

imec

- imec GaN-IC on SOI 200V/ 650V
- imec Si-Photonics Passives+
- imec Si-Photonics ISiPP50G
- imec SiN-Photonics BioPIX 150/ BioPIX 300

IMT

- Glass microfluidics

LioniX International

- LNX SiN-Photonics TriPleX VIS
- LNX SiN-Photonics TriPleX 550
- LNX SiN-Photonics TriPleX 850

MEMSCAP

- MEMSCAP PolyMUMPS
- MEMSCAP SOIMUMPS
- MEMSCAP PiezoMUMPS

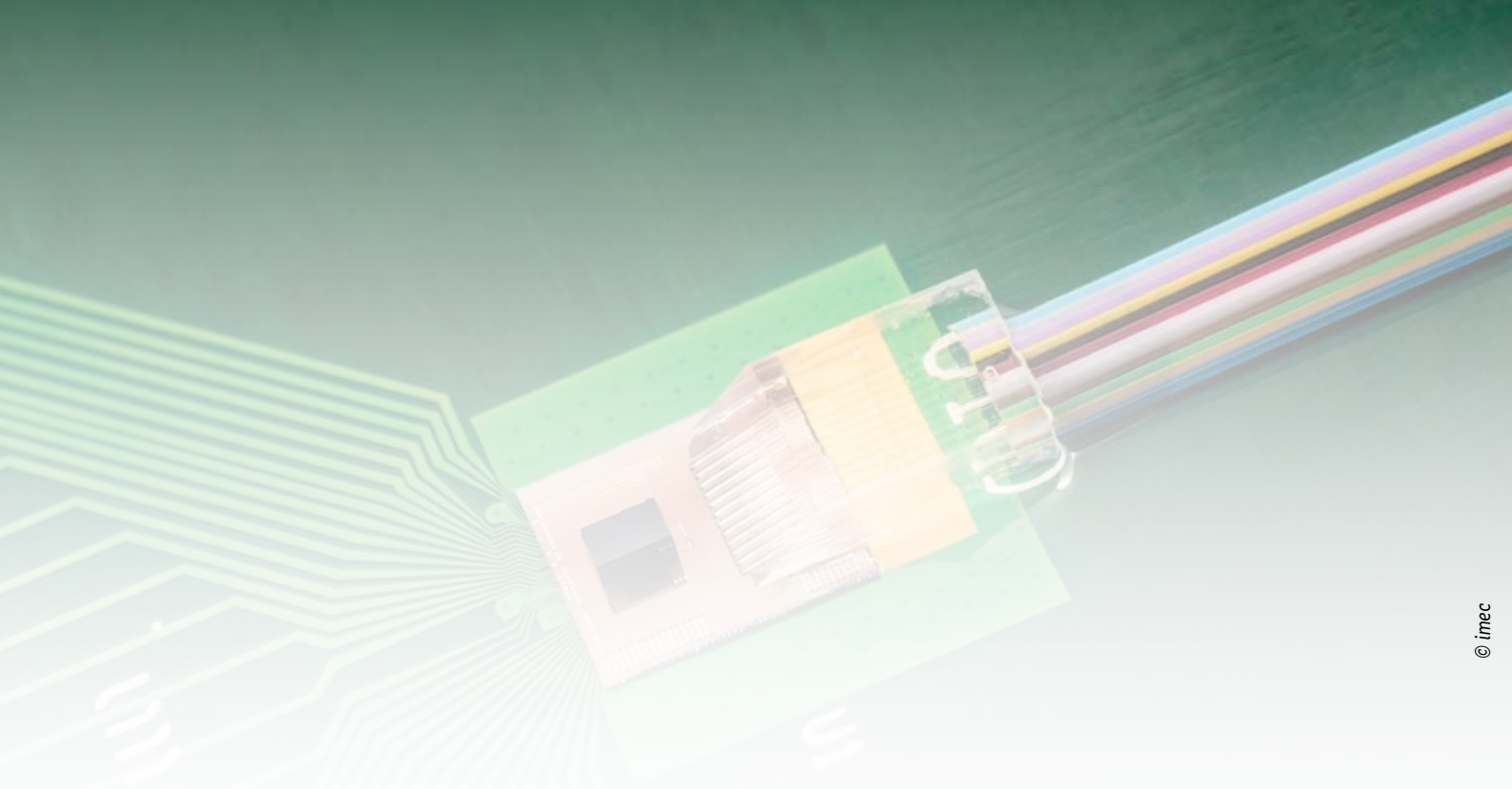
teem PHOTONICS

- Glass-Photonics IC ioNext-NIR
- Glass-Photonics IC ioNext-VIS
- Glass-Photonics IC WAFT

Tyndall National Institute

- PiezoMEMS Single electrode layer stack
- PiezoMEMS Dual electrode layer stack

* 8-inch TSMC technologies will be phased out by the end of 2022. For detailed information and alternatives, please get in touch with your regular EUROPRCATICE contact.



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MULTI-LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi-Level Mask (MLM). With this technique the available mask area (for example 20mm × 20mm field for stepper equipment) is typically divided in four quadrants (4L/R : four layers per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is therefore reduced by a factor of four. By adapting the lithographical procedure, it is possible to use one mask four times for the different layers by using the appropriate quadrants. This technique allows to significantly decrease the mask costs.

The advantages of using MLM single user runs are:

- lower mask costs
- an MLM run is organized for one customer
- it can be scheduled for any date since it does not depend on regular MPW runs
- a customer receives a few wafers, resulting in a few hundreds of prototypes

The MLM technique is preferred over MPW runs when the chip area becomes large and when the customer would like to get a higher number of prototypes. When the prototypes are successful, this mask set can be used under certain conditions for low-volume production.

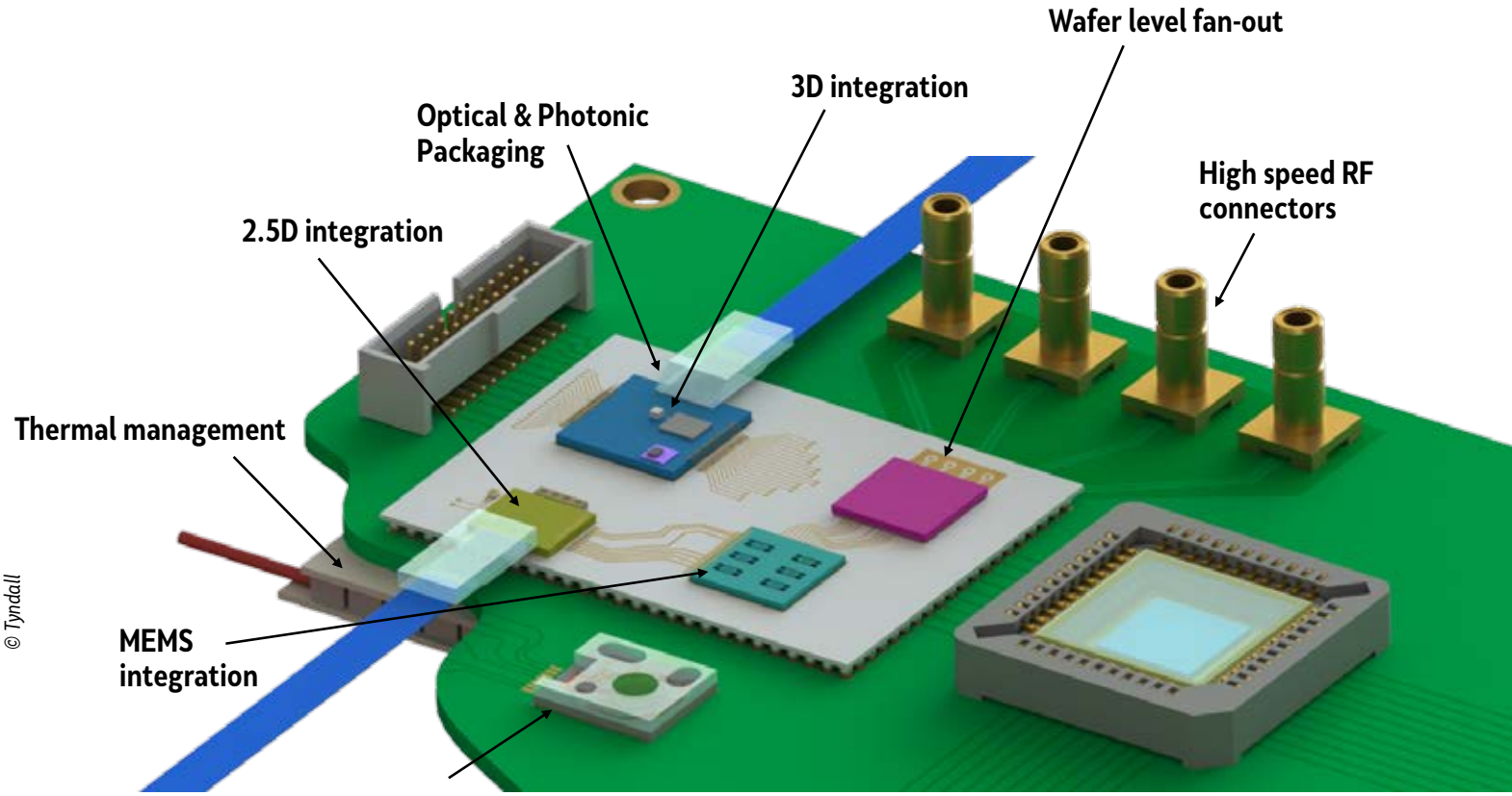
MLM runs are available for technologies from IHP, X-FAB and onsemi. As of 2022, onsemi does not offer MPW runs anymore and focuses on MLM.

PACKAGING

Standardly, EUROPRACTICE delivers unpackaged untested prototypes. However, EUROPRACTICE offers a low-cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of **ceramic and plastic packages** are available, ranging from DILs (Dual-in-line) to PGAs (Pin Grid Array) and QFNs (Quad-Flat No-leads).

Side by side with world class partners and our long-term agreements, EUROPRACTICE boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.

In addition, **photonics packaging** is offered by Tyndall. The photonics ecosystem continues to gather momentum attracting new users (from both academia and industry) and increasing the technical scope of the photonics offering via EUROPRACTICE. Finally, advanced packaging and system integration now complements EUROPRACTICE portfolio.



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VIRTUAL DEMO

ADVANCED PACKAGING AND SMART SYSTEM INTEGRATION

There is a growing demand for advanced packaging and system integration in the semiconductor industry. This trend has been fuelled by the need from a wide range of applications for better integration of more functionalities in a system-on-chip (SoC) and/or system-in-package (SiP). System integration is a scientific and engineering challenge of combining/putting together a variety of technology modules, such as microsystems, microelectronics, optics, photonics, MEMS, microfluidics and combinations of thereof. Examples of system integration in the semiconductor industry are vast, such as high-speed high-density datacom, artificial intelligence (AI), Internet of Things (IoT), bio-medical devices, sensors and many more.

Currently, the EUROPRACTICE portfolio is being extended with advanced packaging and system integration services enabling customers to realize complex multi-technology devices that can be upscaled from early-stage prototypes to volume manufacturing. This is achieved by adding specific processes or technologies in combination with the development of design rules and thereby facilitating advanced package design for system-on-chip integration.

EUROPRACTICE is showcasing the new system integration offer by means of virtual demonstrators, which are depicted on this page. They demonstrate how different building blocks or process modules make integration between multiple technologies possible. This covers advanced packaging of ASICs, photonics, MEMS, microfluidics and combinations of these technologies, from their design to their fabrication and integration.

System integration is made possible through EUROPRACTICE's unique access to a variety of specialized process modules, including 2.5/3D integration of ASICs and PICs through die stacking techniques using pick-and-place, flip-chip, BGAs, Cu pillars as well as silicon interposers. Access to wafer level fan-out packaging is also provided, where dies from different sources or different technologies with varying thickness and size can be handled and packaged with one integration technology. Finally, add-on processes for noble metal finishes and microfluidic building blocks will be added to the technology portfolio, which are prerequisites for many bio-medical sensor devices. Most importantly, all solutions use industry standard processes making them scalable to high volume and more cost effective.

FROM PROTOTYPES TO VOLUME PRODUCTION

Once successful ASIC prototyping has been completed based on the MPW principle, we can also provide a clear route to volume production (from low to mid-high volumes). During this upscaling process, you work closely together with one of the EUROPRACTICE partners, depending on the technology of your choice.

MIGRATION TO A FULL MASK SET

Based on a successful and validated prototype, the ASIC can be fabricated on a dedicated full mask set. One of the EUROPRACTICE partners takes care of the production of the first engineering wafers and organises the assembly in ceramic or plastic packages. Using their own bench tests, the designer can check the functionality of the ASIC produced on the full mask set.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a stable production test program. The test can be performed both on wafer level and on packaged devices. The goal is to screen the ASIC for manufacturing problems using the ATPG (Automatic Test Pattern Generation) and functional patterns. One of the EUROPRACTICE partners supports you during the development of single-site test solution as well as with a multi-site test solution when high-volume testing is required.

DEBUG AND CHARACTERIZATION

Before going into production, a characterisation test program checks if all the ASIC specifications meet the customer's expectations. Threshold values are defined for each tested parameter. The software tests all the IP blocks and functionalities in the ASIC, and the results are validated against the bench test results. A characterisation at Low (LT), Room (RT) and High (HT) temperature is performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be robust against process variations, the product qualification can start. Our partners can support you through the full qualification process using different kinds of qualification flows, including Automotive, Consumer, Industrial, Medical, Space, Military, Jedec and ESCC standards.
In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

YIELD IMPROVEMENT

EUROPRACTICE partners can perform yield analysis to determine critical points during the production and suggest the correct solution to maximise the yield. During the characterisation and qualification of the device on corner lots, the customer receives support in defining the final parameter windows. During the ramp-up phase, data of hundreds of wafers are analysed to check for yield incidents related to assembly and wafer production. The well-proven tool Examinator™ from Galaxy Semiconductor is used, enabling our engineers to perform fast data and yield analysis studies.

SUPPLY CHAIN MANAGEMENT

The responsible EUROPRACTICE partner will manage the full supply chain for you. This highly responsive service takes care of the planning processes with the different actors in the value chain during both engineering and production phases. Integrated logistics ensures the accurate achievement of the final delivery dates.

- **Ceramic assembly partners:** Alter Technology, Kyocera, SERMA Microelectronics, Teledyne e2v
- **Plastic assembly partners:** Amkor Technology, ASE, Greatek Electronics, Integra Technologies, Kyocera, StatsChipPac
- **Wafer bumping partners:** ASE, FlipChip International, Pactech
- **Photonics packaging:** Alter Technology, Bay Photonics, PHIX, PIXAPP, Tyndall
- **Test partners:** Alter Technology, Aptasic, ASE, Bluetest, Delta, EAG Laboratories, Salland Engineering, Microtest, Presto Engineering, RoodMicrotec
- **Failure analysis:** Maser Engineering, RoodMicrotec
- **Library partners:** Aragio, ARM, Cadence, eMemory, Faraday, Synopsys
- **Rad test facility:** LLN, RADEF
- **Tape & Reel:** Reel Service
- **Long-term storage:** HTV

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TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

EUROPRACTICE provides training courses targeting academic staff and PhD students from European universities and research institutes. Unlike training courses which address single topics or individual design tools, the EUROPRACTICE training courses typically address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow.

Since the courses are based on the EUROPRACTICE design tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organization and make full use of the EUROPRACTICE infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants have an opportunity to extensively practice the concepts described in lectures, and have access to experts who can answer questions about the concepts, design tools or technology processes discussed on the course.

Where a design flow is well supported by multiple vendors and/or processes, multiple course variants are offered that reflect the typical practice within European industry.

Since EUROPRACTICE Training courses began in April 2014, a total of 1551 delegates from 316 Member Institutes in 40 countries have attended 174 training courses making 5391 days of practical training.

Due to the COVID-19 pandemic, physical training courses were reconfigured and adapted so they could be presented online as live instructor-led training including hands-on practical sessions using remotely accessible design tool environments.

WEBINARS

To introduce the constantly growing service portfolio and share valuable technology insights, EUROPRACTICE regularly develops and hosts highly successful webinars. These online events usually include informative presentations given by experts from world-leading companies, foundries or academic institutions, followed by a short Question & Answer session. All webinars are free of charge and open for a broad audience with different background.

In 2020, three very popular webinar series took place: Advanced Photonics Packaging, Introduction to Microfluidics, and Silicon-Photonics. Over the past year, we have hosted three more equally successful series with a total of 10 episodes:

Recordings of all our webinars are available on the official YouTube channel of EUROPRACTICE Services.

Together with webinar series, EUROPRACTICE also hosts single-episode sessions. The two following webinars can serve as examples of such events in 2021:

- Lowering the Barrier for Customized Microsystems in Medical Applications, organised by EUROPRACTICE together with DSP Valley and flandrs.health,
- Introduction to Multi-Project Fan-out Wafer Level Packaging (FOWLP) by Fraunhofer IZM.

Since the very first webinar, which took place at the end of 2019, all EUROPRACTICE webinars have remained highly popular: 31 live-stream sessions were attended by 2565 delegates, followed by around 20000 views of the recordings on YouTube.

For 2022, various new webinars are being planned. For instance, a series on Smart System Integration is currently under development.

Introduction to MEMS Technologies

This series was prepared by experts from Tyndall and imec to make participants better acquainted with Micro Electro Mechanical Systems (MEMS). The first introductory webinar was followed by three episodes that provided an overview of MEMS fabrication services available through EUROPRACTICE, including technologies of X-FAB, MEMSCAP and Tyndall.

Flexible Electronics

This three-webinar series was designed to introduce the EUROPRACTICE community to the world of flexible electronics and, more importantly, to trigger the interest of our customers for technologies that will become accessible in the near future. The series started with an introduction to the flexible technologies and their applications, then it focused on the offer of PragmatIC and QUAD Industries.

Introduction to imec's MPW Services

EUROPRACTICE lowers the entry barrier to imec advanced process technologies available in the MPW mode. The series consists of three episodes, where each session is dedicated to one of the following imec technologies: Si-Photonics, SiN-Photonics and GaN-IC. The webinars took place in January-February 2022.

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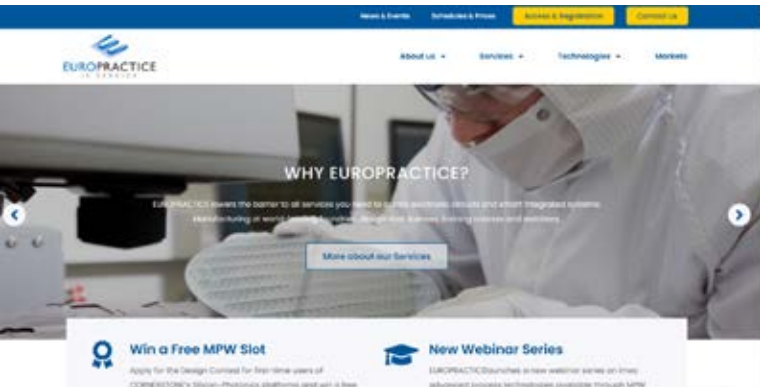
OUTREACH AND COMMUNICATION

The past two years have been very challenging for communication and outreach activities since the majority of face-to-face events have been cancelled due to COVID-19 restrictions. To remain in touch with our customers and reach new users, EUROPRACTICE has actively used virtual tools, such as websites, social media, and online events.

WEBSITES

Information on a very broad and diverse EUROPRACTICE offer is split between three websites that cover different aspects of the service portfolio. In 2021, we restyled and restructured all the websites to make the navigation more intuitive and the overall experience more user-friendly.



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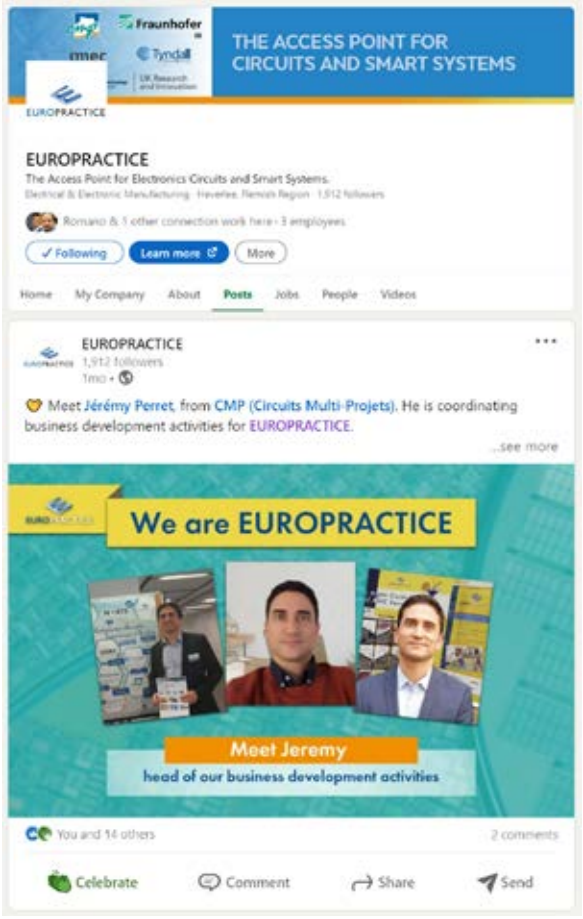
europractice-ic.com : The Technology & Fabrication website is regularly updated by imec with the latest news on MPW offer, run schedules and pricing. Here visitors can find all information related to fabrication process, including detailed technology descriptions, packaging offer, system integration solutions and volume production services. Last year, the website was made more application and market oriented to become more accessible for industrial customers.

europractice.stfc.ac.uk : The Design Tool & Training website is hosted and maintained by UKRI-STFC. It presents information related to EUROPRACTICE membership, purchase of design-tool licenses, upcoming training courses and webinars. Thanks to the refreshed style, we achieved considerable improvements in the presentation of the offer and the user experience.

europractice.com : This website gives new customers a general overview of the EUROPRACTICE services. It helps to redirect them to the first two major websites.

SOCIAL MEDIA

To enlarge and strengthen the EUROPRACTICE user community, we actively develop accounts on LinkedIn and YouTube. By the end of 2021, we managed to create a strong presence in both social networks.



LinkedIn

Following EUROPRACTICE on LinkedIn is an effective way for customers to receive most relevant news. In December 2021, our official LinkedIn account had close to 1900 followers.

YouTube

The YouTube channel of EUROPRACTICE Services gives a great opportunity to watch all our webinars. By the end of 2021, the channel had around 20000 views and more than 540 subscribers.

EVENTS IN TIMES OF COVID-19

Before the COVID-19 restrictions, EUROPRACTICE partners were regularly present at various scientific conferences, industrial trade shows and fairs to present our services to existing customers and to attract new prospects. In 2021, most of such events took place in an online format. EUROPRACTICE took part in several of them with a virtual booth. However, this format made interaction with other participants less efficient.

To improve outreach, we have tried different types of online communication. For instance, EUROPRACTICE partners organised a panel discussion at ESSCIRC-ESSDERC2021, which proved to be more successful than a virtual booth. Six panellists form leading microelectronics organisations have shared their opinion about the role of EUROPRACTICE in the European microelectronics ecosystem. In addition, two online industry-cluster events were co-organised with DSP Valley and Silicon Saxony respectively.

To compensate for the lack of face-to-face interaction opportunities, EUROPRACTICE has been successfully using online communication channels, such as webinars and social media. In the next years, we will keep benefiting from them. In 2022, we will attend at least the following conferences and fairs:

Banner advertising the EUROPRACTICE panel discussion at ESSCIRC-ESSDERC 2021.

LinkedIn invitation to visit the EUROPRACTICE virtual booth at EFECS 2021.

Screenshot of the EUROPRACTICE virtual booth at ISSCC 2021.

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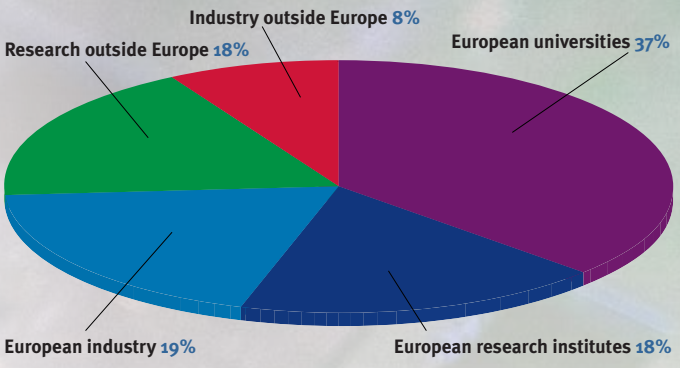
ISSCC 2022	Virtual event	20-24 February
SSI 2022	Grenoble, France	26-28 April
PRIME 2022	Villasimius, Italy	12-16 June
ESSDERC / ESSCIRC2022	Milan, Italy	19-22 September
EFECS 2022	Amsterdam, the Netherlands	24-25 November

RESULTS 2021: MPW PROTOTYPING SERVICES

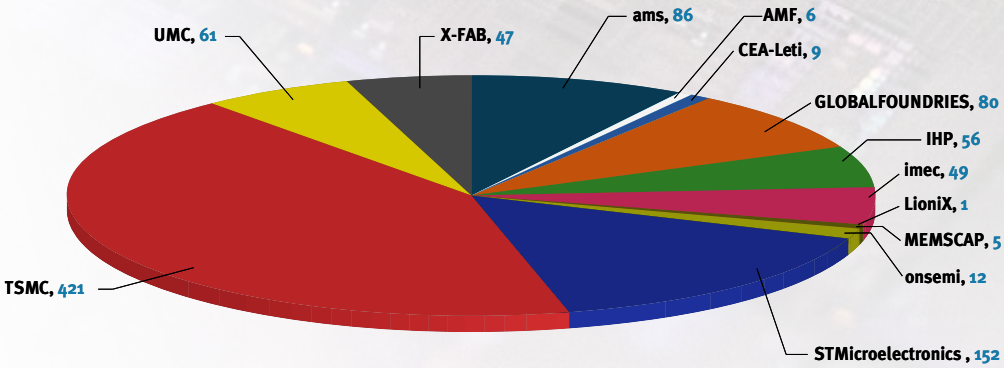
PROTOTYPED CIRCUITS ON MPW RUNS

In 2021, a total of 985 designs were submitted for prototyping on EUROPRACTICE MPW runs, which is 10 percent more compared to the previous year. This significant growth reflects the increased demand in the global semiconductor market. It also shows that the EUROPRACTICE MPW offer successfully meets customers' needs and allows the service to continue effectively supporting European academia and industry.



MPW designs in 2021

European customers submitted the vast majority of the designs (74%). 55% of all the prototypes fabricated in 2021 were designed by universities and research institutes located in Europe, while 19% came from the European industry, mainly from SMEs and startups. The remaining 26% of the designs were developed in other regions.

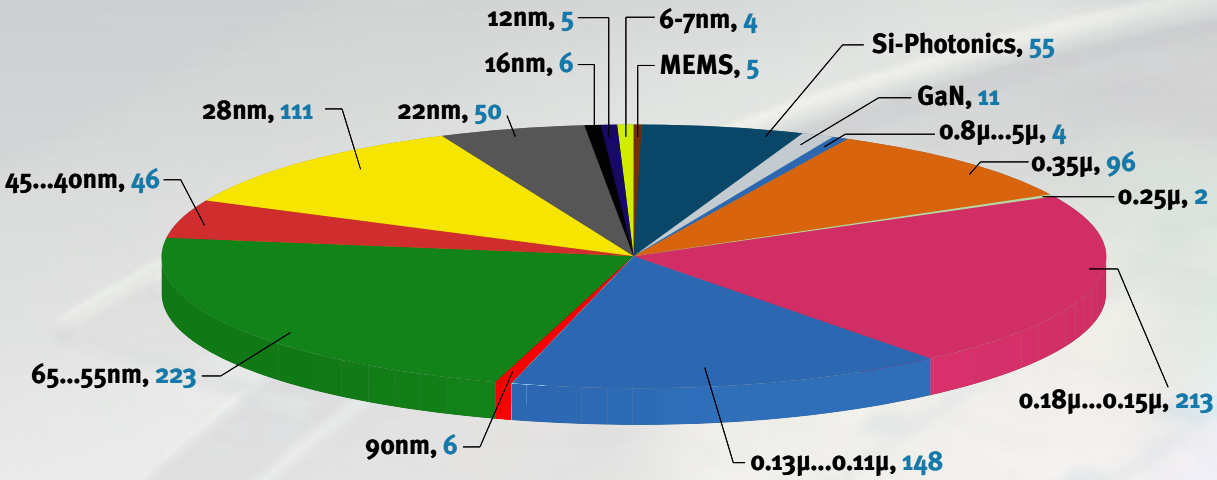


Number of fabricated designs in 2021 per foundry

ACCESS TO TECHNOLOGIES OF WORLD-LEADING FOUNDRIES

EUROPRACTICE provides affordable access to technologies of world-leading foundries (ams, GLOBALFOUNDRIES, STMicroelectronics, TSMC, UMC and X-FAB), complemented by R&D fabs, such as CEA-Leti, IHP and imec. Like previous years, most of the submitted designs in 2021 were fabricated in TSMC, the leading foundry for the global industry.

Remarkably, two European foundries – STMicroelectronics and ams – have the second and third largest number of fabricated designs. They are followed by another world-leading foundry, GLOBALFOUNDRIES, which nearly doubled its share of designs compared to the previous year. European R&D fabs, including CEA-Leti, IHP and imec, also have a significant number of prototypes. Finally, the first design in a LioniX International technology was submitted in 2021.



Number of fabricated designs in 2021 per technology (node)

GOOD TECHNOLOGY MIX

EUROPRACTICE offers a good technology mix to its customers. As you can see on the pie chart, advanced technologies, older technology nodes and More-than-Moore technologies are all used in significant volume.

The older technology nodes (ranging from 0.11µm to 0.5µm) are still very popular and represent approximately half of the submitted designs. For more advanced nodes, 65nm and associated nodes are the most popular, with 223 fabricated prototypes.

Finally, advanced technologies in the EUROPRACTICE portfolio were more frequently used in 2021 compared to the previous year. For instance, the number of designs in both FDSOI technologies – ST28FDSOI and GF22FDSOI – has grown from 23 in 2020 to 84 last year. We can also see a significant increase in the number of FinFET prototypes manufactured at GLOBALFOUNDRIES and TSMC, with nodes ranging from 16 to 6 nm.

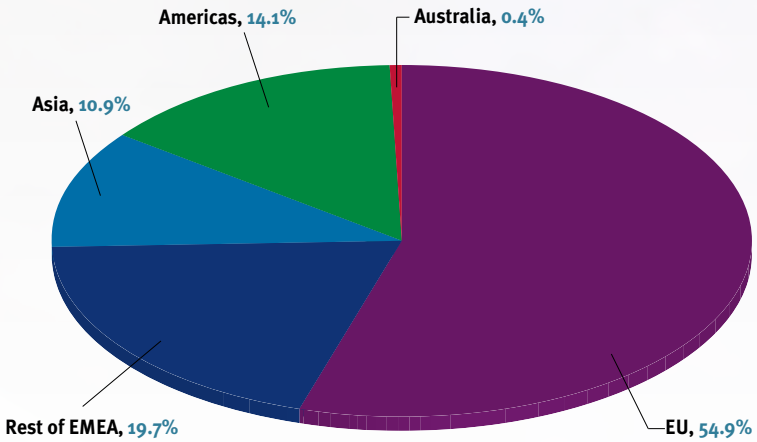
In 2021, 55 Silicon-Photonics designs were registered, which is 20 percent more than the previous year. We can attribute this growth to extending the EUROPRACTICE Photonics portfolio by including new foundries and technologies. In addition, we see an increase in the number of prototypes in GaN-IC: It rose from 2 in 2020 to 11 last year, indicating the growing popularity of this technology.

GEOGRAPHICAL DISTRIBUTION

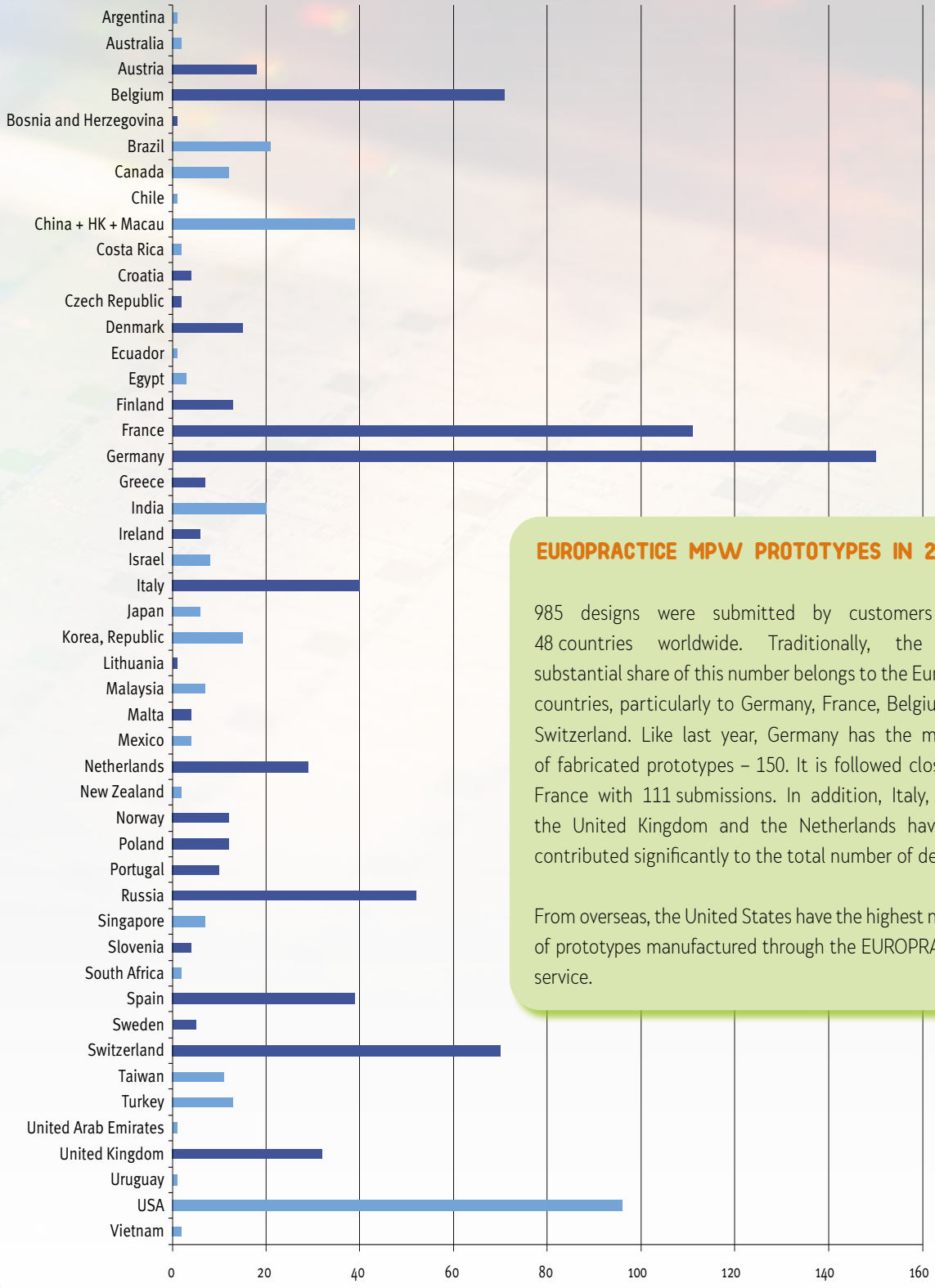
EUROPRACTICE focuses mainly on European customers, therefore 74% of the fabricated designs in 2021 are coming from Europe and the EMEA (Europe, Middle East and Africa) zone.

A moderate number of customers from Asia also used the EUROPRACTICE prototyping services last year, representing a total volume of 107 designs.

Finally, the remaining 15% of the manufactured prototypes are coming from the Americas and the Australian continent.



Geographical distribution of MPW designs in 2021



EUROPRACTICE MPW PROTOTYPES IN 2021

985 designs were submitted by customers from 48 countries worldwide. Traditionally, the most substantial share of this number belongs to the European countries, particularly to Germany, France, Belgium and Switzerland. Like last year, Germany has the majority of fabricated prototypes – 150. It is followed closely by France with 111 submissions. In addition, Italy, Spain, the United Kingdom and the Netherlands have also contributed significantly to the total number of designs.

From overseas, the United States have the highest number of prototypes manufactured through the EUROPRACTICE service.

USER STORIES ON PROTOTYPED DESIGNS

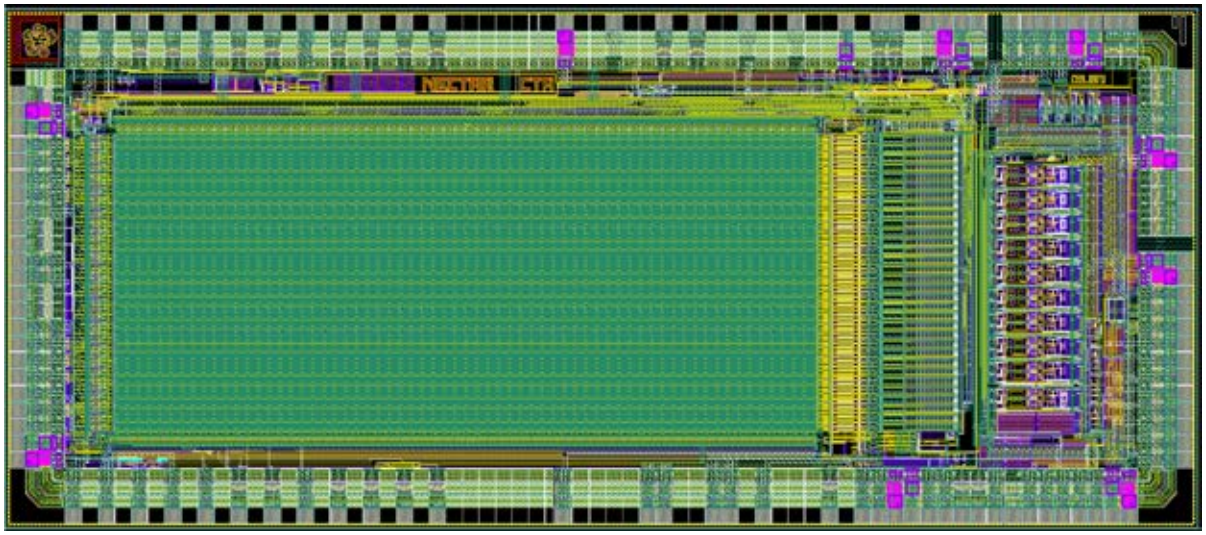


Fig.1: Layout of the NECTAR3 chip.

NECTAR3: 12-bit digitizer for the Cherenkov Telescope Array (CTA)

CEA-Saclay, DRF IRFU, Gif Sur Yvette, France

Contact:	Delagnes Eric
E-mail:	eric.delagnes@cea.fr
Technology:	ams 0.35µm CMOS C35B4C3
Die size:	7160µm x 3080µm
Application Area:	High Energy Physics (HEP)

Introduction

Within the framework of the CTA 5cerenkov Telescop Array) observatory, our initial need was to digitize more than 20,000 very high frequency channels (> GSPS) with a dynamic range of about 15 bits. At the beginning of the project, such a low power digitizer did not exist commercially and especially not at a reasonable cost. The NECTAR circuit, developed in ams CMOS 0.35µm technology, and resulting from R&D conducted for other projects since 2005, has made it possible to meet this demand.

Description

The NECTAR3 circuit is a 12-bit digitizer with a sampling rate of up to 3GSPS. Each of its 2 channels is composed of an analog memory with a depth of 1024 which is frozen and digitized by an ADC pipeline (20MSPS) when a trigger signal arrives. The main difference with the previous generation "NECTAR" is the possibility to split the memory into two parts of 512 points used in ping-pong mode. One part stores the signal, while the other part, containing the previous event, is digitized.

For our application on CTA (random event rate up to 10kHz), this allows to reduce the dead time by more than one decade.

Results

Because of the delays related to the plastic packing of this chip (made by another company) , this final version of the circuit has not been tested yet. Nevertheless, we can say that the tests on the previous prototype of the circuit have demonstrated the capability offered by the new architecture to decrease the deadtime. This prototype chip was fulfilling all our requirements. On the version submitted in this run, which is actually a production run, only second order improvements have been made. We are now waiting the first batch of 12000 packaged chips that will be tested before to be sent to the company that will mount them on boards.

Why EUROPRACTICE?

CMP has been a reliable partner for more than two decades. We appreciate the flexibility they offer for prototyping while respecting confidentiality. The possibility offered by CMP to remanufacture old designs in medium volumes at reasonable cost is also very important to us.

Low-power acoustic wake-up receiver (WuRxs) for underwater applications

Department of Microsystems (IMS),
University of South-Eastern Norway, Norway

Contacts:	Arian Nowbahari, Luca Marchetti, Mehdi Azadmehr
E-mail:	arian.nowbahari@usn.no
Technology:	ams 0.35µm CMOS C35B4C3
Die size:	3mm x 3mm
Design Tools:	Cadence
Application Area:	IoT

Introduction

Underwater wireless sensor networks (UWSNs) are implemented in different applications such as: ocean monitoring, offshore exploration and disaster prevention. An UWSN consists of many sensor nodes (up to thousands), generally supplied by a small battery. The sensor nodes acquire data, manipulate them and send back to a base station. The most critical issue is the system energy efficiency. To reduce the overall power consumption, and so to extend the UWSN lifetime, wake-up receivers (WuRxs) are typically implemented. The WuRxs activate the sensor nodes only when communication is required, avoiding problems such as idle listening and overhearing. Idle listening occurs when sensor nodes are listening to a channel but no data is transmitted over it. Instead overhearing occurs when a sensor node receives a packet of data not intended to it. WuRxs can solve these issues, since they activate the network components on demand.

Description

We designed a low-power acoustic wake-up receiver for underwater applications. Our system is composed of a water tank, two transducers, and the fabricated device (Figure 1). On the TX side a transducer sends a certain wake-up call code, which consists of a well-defined sequence of bursts. On the RX side a transducer converts the acoustic bursts into an electrical signal. The fabricated device decodes the incoming signal, and if the latter resembles the wake-up call it activates the sensor node.

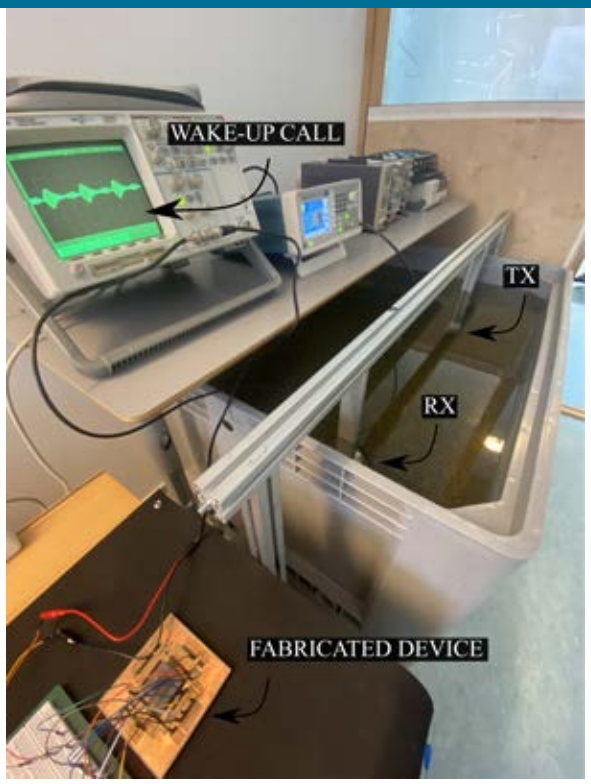


Fig.1: Experimental setup for testing the acoustic underwater wake-up receiver.

Results

The fabricated WuRx has been shown to be functional: it generates an interrupt signal when the correct wake-up call is received. Before chip fabrication the device has been proved to be functional only at simulation level [1, 2]. Therefore, the preliminary measurements validated our prototype. In the future we plan to test the fabricated device in the ocean. The device is low-power with State-Of-The-Art power consumption.

Why EUROPRACTICE?

We use EUROPRACTICE because all the steps of the ASIC fabrication are excellently managed: from the design step to the packaging one. Moreover, EUROPRACTICE allows us to realize prototypes at reasonable academic prices.

Acknowledgements

The authors thank EUROPRACATICE MPW and design tool support for ASIC fabrication.

References

[1] Nowbahari, L. Marchetti and M. Azadmehr, "An Ultra-Low Power Multivibrator-Based Wake-up Receiver for Wireless Sensor Networks," 2021 IEEE 7th World Forum on Internet of Things (WF-IoT), 2021, pp. 380-384, doi: 10.1109/WF-IoT51360.2021.9595159.

[2] A. Nowbahari, L. Marchetti and M. Azadmehr, "A Delay-Based Wake-Up Receiver for Wireless Sensor Networks," 2021 International Conference on Electrical, Communication, and Computer Engineering (ICECCE), 2021, pp. 1-5, doi: 10.1109/ICECCE52056.2021.9514246.

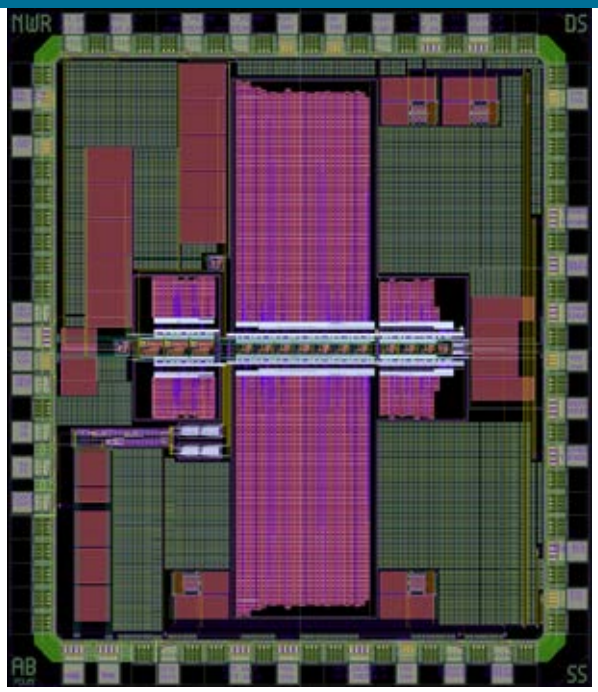


Fig.1: Layout of the fabricated circuit.

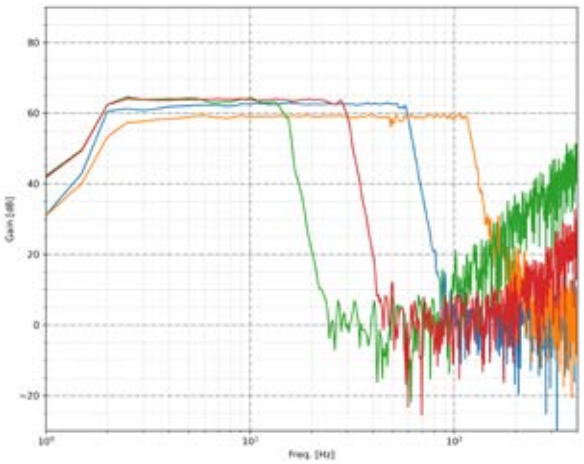


Fig.2: Test result depicting Gain [dB] vs Frequency [Hz].

A switched-capacitor front-end for neural sensing

Newronika S.p.A., Italy

Contacts:	Sergio Sinisi, Andrea Bonfanti
E-mail:	sergio.sinisi@newronika.com
	andrea.bonfanti@polimi.it
Technology:	ams 0.35µm CMOS C35B4C3
Die size:	2548µm x 2968µm
Application Area:	Medical / Health

Introduction

This device is intended to be used in Deep Brain Stimulation (DBS) applications. DBS is used for the treatment of neurological disorders, as Parkinson's Disease, Dystonia and Essential tremors. A natural path for the improvement of this technique is to chronically observe the stimulation effects on the neurophysiological response. This requires a circuit able to acquire the low-frequency signals coming from the brain, in presence of strong out-of-band interferences due to deep-brain stimulation, in a robust and reliable fashion. Here we present the architecture and the design of an integrated circuit able to perform artifact-free recording of neural signals.

Description

The circuit implements the front-end electronics to acquire Local Filed Potentials (LFPs) in the frequency range from 1Hz to 100Hz from the brain of patients affected by Parkinson's disease. The main goal of this system is to register the signal of interest at low noise (<1 µV) while rejecting the artifacts due to the deep brain stimulation (DBS), which involves the injection of high-current pulses (in the range 1-10mA) at 130 Hz. The circuit implements a 7-th order switched-capacitor Cauer filter with an adjustable low-pass cut-off frequency from 10Hz to 100Hz and able to reject the stimulation artifact at 130Hz by more than 70dB. The filter is followed by a 3-rd order Sigma-Delta A-to-D converter to process the neural signal in the digital domain.

Results

The whole front-end including amplifier, filter and A-to-D converter draws a current of 100uA from a 3-V power supply. The in-band gain is 60dB and the low-pass cut-off frequency can be digitally selected to 12Hz, 25Hz, 50Hz and 100Hz. The input noise power spectral density is smaller than 100nV/sqrt(Hz), leading to a minimum signal that can be acquire as small as 1 µV. The stimulation artifact at 130Hz is rejected by more than 70dB in the worst-case (low-pass filter frequency of 100Hz). This allows to correctly acquire the feeble neural signal (Local Field Potential) even in presence of a differential artifact of 100mV.

Why EUROPRACTICE?

Yet another positive experience with CMP / EUROPRACTICE services that we would recommend for ASIC prototyping and low volume production.

Acknowledgements

We would like to thank Daniel Senderowicz for his huge contribution in the design of the test-chip.

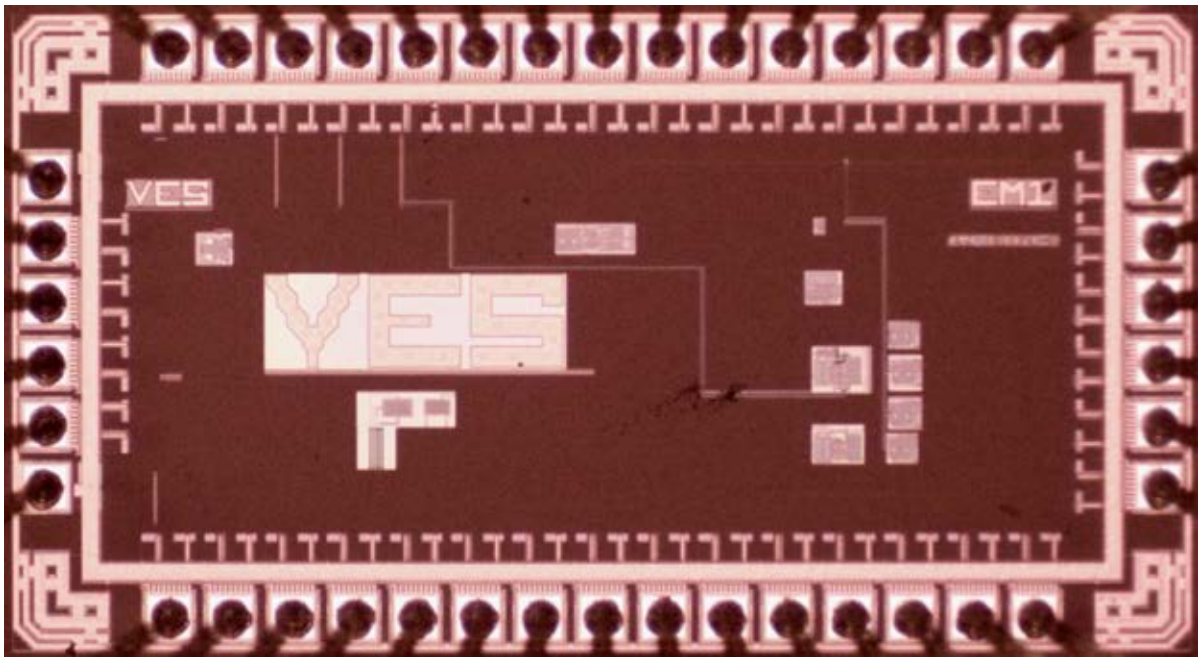


Fig.1: Die shot of the manufactured Chip.

Integrated oscillator and amplifier for biomedical devices

Christian-Albrechts-Universität zu Kiel, Networked Electronic Systems, Kiel, Germany

Contacts:	Robert Rieger, Sebastian Simmich, Patrick Wiegand
E-mails:	rri@tf.uni-kiel.de, ssi@tf.uni-kiel.de, pw@tf.uni-kiel.de
Technology:	EM Microelectronic EMALP018
Die size:	1906µm x 1026µm
Design Tools:	Cadence Virtuoso
Application Area:	Medical / Health

Introduction

With more sophisticated means of measuring heart and brain activity by magnetic fields, magnetic sensors need to get small and sensitive enough for biomedical signals. Delta-E effect sensors show the potential to match these criteria. This IC provides an oscillator and a dual-channel low-noise amplifier to excite and read out these sensors. The oscillator excites a cantilever-type sensor at its frequency of resonance and the amplifier buffers the modulated sensor signal for further processing.

Description

On this chip, a ringoscillator as well as a two-channel current-reuse amplifier is implemented. The ringoscillator is connected to a two-pole low-pass filter to suppress higher harmonic frequencies and selectively pass the fundamental frequency, providing a sinusoidal output to drive the sensor at its resonance frequency. The oscillator frequency, amplitude and offset voltage are tunable to meet different sensor's needs.

The amplifier is designed to achieve low-noise operation and a unity-gain bandwidth of above 1 MHz. It employs a current-reuse topology in which input stages are stacked to reuse the bias current and thus conserve energy.

Results

The implemented ringoscillator is frequency and amplitude adjustable between 0.5 MHz and 2 MHz and 100 mV to 350 mV, respectively. By low-pass filtering with a cut-off frequency of 1 MHz and using the implemented 2nd-order filter, higher harmonics are successfully suppressed. Within this frequency range, the current-reuse amplifier provides a gain of 10 dB and input-referred spot voltage noise well below 50 nV/ √Hz.

Why EUROPRACTICE?

CMP / EUROPRACTICE provide a clear and easy-to-use web interface for design registration, submission, and queries. The staff is supportive, knowledgeable and easy to contact. The research group has been satisfied with CMP / EUROPRACTICE's services for many years.

Acknowledgements

This research was funded by the German Research Foundation (DFG) via the collaborative research center CRC 1261.

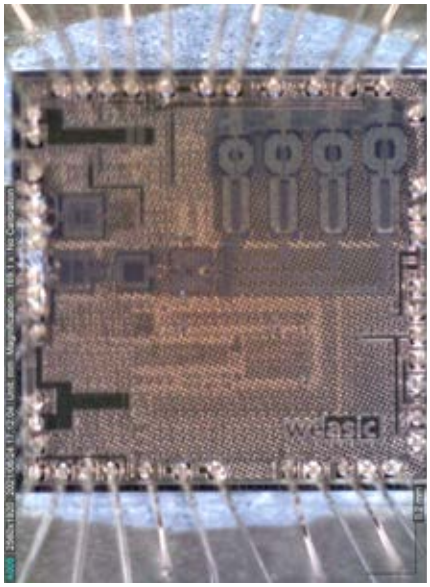


Fig.1. Chip picture of the QFN package with the die.

Fig.2. PLL 7GHz measured performance with reference operating at 200MHz (2 X 100MHz external reference).

Fractional-N RF synthesizer for 5G backhaul and satellite communications

Weasic, Greece

Contact:	Weasic's Team
E-mail:	gkamoul@weasic.com
Technology:	GLOBALFOUNDRIES 45nm RFSOI
Die size:	1.6mm X 1.6mm
Application Area:	Datacom / Telecom

Introduction

The expanding market of 5G backhaul networks and the growing demand for satellite communications both lead to an increasing customer need for high-performance wideband synthesizers. These two factors have weigh on our decision to develop a family of Fractional-N RF Synthesizers to address those markets. Leveraging customer feedback and proprietary data collected from the field, we have come to the conclusion that the Fractional-N RF Synthesizer market for 5G backhaul and satellite radios is a worth-making investment for Weasic with significant expected ROI.

Description

The device is a Fractional-N RF synthesizer with a wide output frequency range from 7GHz to 28GHz, low output phase noise -100dBc at 100KHz offset (when output is 14GHz) and -92dBc at 100KHz (when output is 28GHz). The system requires a reference signal of 100MHz to 800MHz and provides an output signal with power greater than 0dBm across the frequency range. The device is fabricated with 45RFSOI, a partially depleted SOI technology of GLOBALFOUNDRIES.

Results

We have verified the full functionality of the PLL. The measured results are quite close to the simulated performance. This device can be used as a low power PLL for demanding applications like 5G backhaul & Satellite comms where there is a great need for mmWave LO signals that can be phase adjusted over time.

Why EUROPRACTICE?

We have used the EUROPRACTICE Services in order to submit the design in the GF 45RFSOI process. With the help of EUROPRACTICE, we managed to deliver a DRC free design and integrate our PLL design into a 36pin QFN package. Throughout the overall process, EUROPRACTICE Services have been very helpful and provided guidelines in order to support us in all the chip processing steps from GDSII DRC verification up to the packaging of our PLL project.

Acknowledgements

We would like to thank GLOBALFOUNDRIES and especially Ned Cahoon for supporting us all the way.

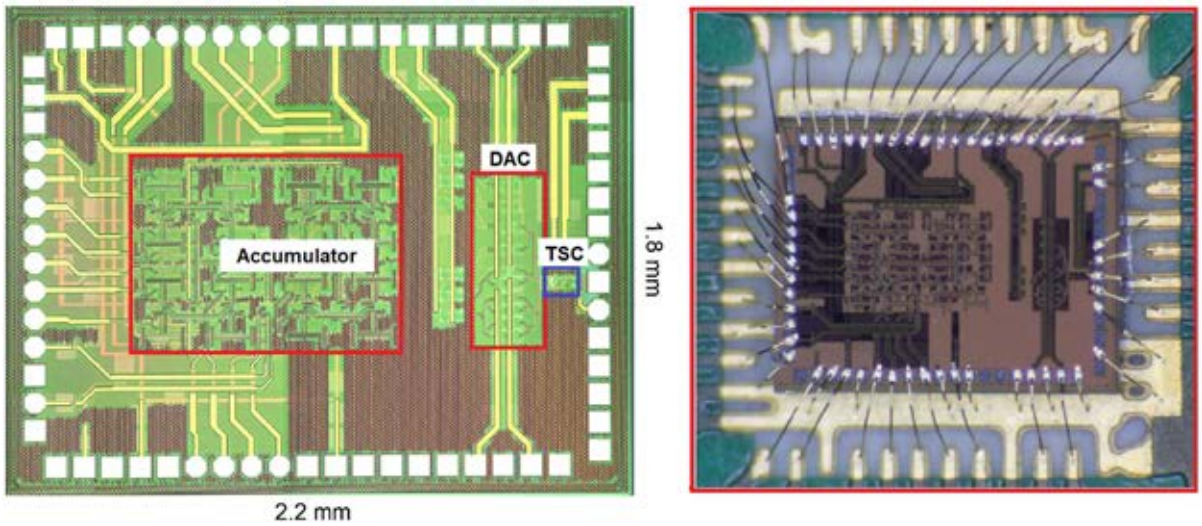


Fig.1: Die micrograph of fabricated DDS chip (left) and wirebonded chip (right).

SiGe based ROM-less 18.5 GHz Clock Direct Digital Synthesizer

Goethe University of Frankfurt am Main, Germany

Contacts:	Amit Shrestha, Eugen Dischke, Viktor Krozer
E-mail:	shrestha@physik.uni-frankfurt.de
Technology:	IHP 0.25µm SiGe BiCMOS SG25H4
Die size:	2200µm x1800µm
Application Area:	Datacom / Telecom

Introduction

The direct digital synthesizer (DDS) has significant advantages over the conventional phase-locked loop (PLL) based analog synthesizers for microwave frequency synthesis in terms of wide output frequency range, fast frequency hopping, modulation capabilities, compact size, and low phase-noise.

Description

We have designed a full DDS in ROM-less architecture to be operated at clock frequencies approaching 20 GHz in SiGe technology. It consists of 12-bit Phase accumulator, additional 6-bit phase control, 6-bit Digital to analog converter (DAC), and analog TSC. We used the SG25H4 technology due to its speed and maturity.

Results

The DDS is fabricated in IHP 0.25µm SG25H4 SiGe BiCMOS technology is shown in Figure 1 (left). The wire-bonded DDS chip on PCB is shown in Figure 1 (right). The chip micrograph highlighted different blocks (accumulator, DAC and TSC). The DDS die area is 3.96 mm2 with 59 pins, and the total power consumption is 1.5 W. The total number of transistors used in this design is ~ 4500. The accumulator occupies 40% of the total chip area and consumes 80% of total power consumption.

The DDS is measured for various FCW inputs for a fixed (maximum) clock of 18.5 GHz. Up to 5 GHz output, the SFDR and output power level are at least 15 dBc and -18 dBm respectively. The phase noise characteristics of the 3 GHz DDS output is better than –115 dBc/Hz at 1 KHz offset from the carrier.

Why EUROPRACTICE?

EUROPRACTICE offers access to special technologies, such as the IHP 250nm BiCMOS process. Further EUROPRACTICE staff provides technical know-how and aids the designers through the tapeout and other associated processes. We were very pleased with the service offered by EUROPRACTICE team.

Acknowledgements

The authors gratefully acknowledge the financial support of this research by the RAMMS project (03SX422B) and MIMIRAWE project (50RA1326).

Extreme broadband and reconfigurable integrated photonic electronic receiver on silicon substrate

Institute of Electrical and Optical Communications Engineering, University of Stuttgart, Germany

Contacts:	Jakob Finkbeiner, Niklas Hoppe, Philipp Thomas, Christian Schweikert
E-mail:	jakob.finkbeiner@int.uni-stuttgart.de
Technology:	IHP SG25H5_EPIC
Die size:	2.5mm x 2.1mm
Design tools:	RSoft, PhotonDesign, Cadence Virtuoso, Spectre, ADS Momentum
Application Area:	Datacom / Telecom

Description

Exceptionally high transmission capacities of optical communication systems can only be exploited by using electronic circuits in parallel, since the bandwidth of electronic circuits is fundamentally limited by the transit frequency of the available transistors. The developed electronic photonic integrated circuit (EPIC) enables extreme broadband and reconfigurable receivers on a single chip via photonic preprocessing followed by time interleaving electronic demultiplexing.

In common communication systems, the wide optical band with a spectrum in the THz range is subdivided into many small frequency bands (wavelength division multiplexing, WDM). The superimposed wavelength channels can be spectrally separated in the developed receiver by an integrated arrayed waveguide grating filter (AWG). Additional optical phase shifters in intermediate coupling structures of multimode interference couplers (MMIs) can select and route a specific wavelength channel. The conversion of the analog optical signal to a digital electronic signal is usually limited by the bandwidth of the analog-to-digital converters (ADC). To take full advantage of the large bandwidth of photodetectors and transimpedance amplifiers, an integrated 1:4 100 GBaud current demultiplexing circuit enables the parallel use of low-bandwidth ADCs. The monolithic approach chosen avoids any parasitic packaging inductance and capacitance that would reduce the bandwidth.

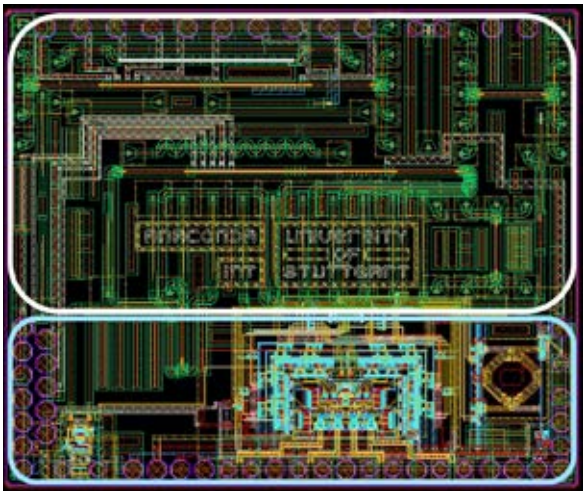


Fig.1: Layout of the designed device depicting the photonic circuit (top) and the electronic circuit (bottom).

On the top part of Figure 1, we see the layout of the Photonic Circuit including grating coupler array, 90° hybrid, optical switching network and photodiodes. The bottom part shows the Electronic Circuit including transimpedance amplifier and demultiplexer.

Simulations have shown that the designed optoelectronic front end, consisting of photodiodes, transimpedance amplifier, and demultiplexer can sample 100 GBaud NRZ and 50 GBaud PAM4 optical signals, corresponding to a total data rate of 100 Gb/s. The developed optoelectronic circuits could potentially be used in future transceivers in data centers to realize a monolithic, broadband and flexible receiver. Delivery and measurement of the EPIC chip is scheduled for December 2021.

Why EUROPRACTICE?

As a research institute specialized in the design of integrated electronic and photonic circuits, quick and easy access to leading design tools and state-of-the-art semiconductor technologies is critical to us. We rely on EUROPRACTICE for software licensing, design kit access, training courses and particularly IC fabrication in some of the most advanced semiconductor technologies. We greatly appreciate the benefits of participating in the EUROPRACTICE program and are very grateful for the technical support provided by EUROPRACTICE.

Acknowledgement

This work was supported by the German Research Foundation within the Priority Program SPP2111: Electronic-Photonic Integrated Systems for Ultrafast Signal Processing under Grant BE2256/34-1.

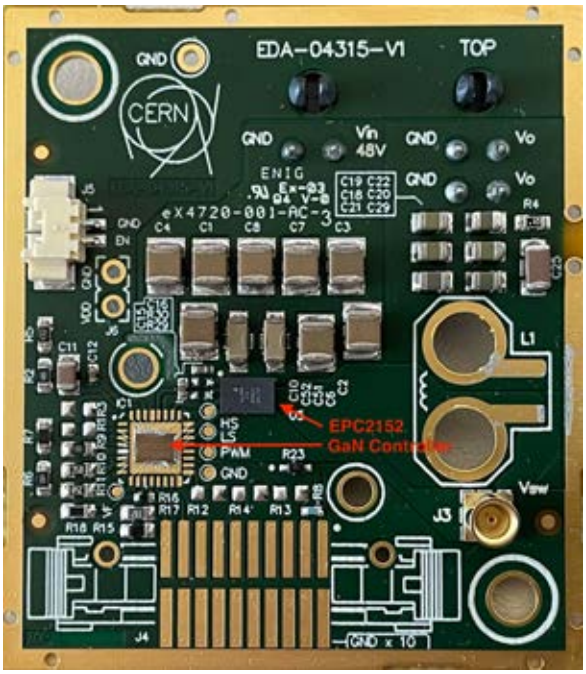


Fig.1: bPOL48V board hosting Gan_Controller and EPC2152.

bPOL48V: a rad-hard 48V to 12V DCDC converter

CERN, Switzerland

Contacts:	Stefano Michelis, Pablo Antoszczuk
E-mail:	stefano.michelis@cern.ch
Technology:	onsemi I3T80
Die size:	2500µm x 3000µm
Application Area:	High Energy Physics (HEP)

Introduction

In the past, a compact, rad-hard and efficient power distribution strategy for High Energy Physics (HEP) detectors has been developed, whose strategy is based on a 12V bus that is locally stepped down using two stages of Point-of-Load DCDC converters. The first-stage converters (bPOL12V) create a 2.5V domain, which powers the opto-electronic components, while the second-stage converters (bPOL2V5) step down the voltage from 2.5V to supply the front-end analog and digital circuits. bPOL12V and bPOL2V5 are today in production for HL-LHC experiment upgrades.

Due to the distance between the off-detector power supplies and the first stage converters, the power dissipation, cost and weight of the wiring and power supplies are significant. One strategy to reduce the requirements of the power distribution scheme is to rise the bus voltage to 48V, with the consequent reduction on the current required to deliver a given power, and step down the larger bus voltage to the intermediate 12V bus as close as possible to the first-stage converters.

A rad-hard DCDC converter from 48V to 12V called bPOL48V has been developed, with the control circuit who is the object of this user story, called GaNController, designed in the onsemi I3T80 technology and the power stage using the EPC2152 chipset based on Gallium Nitride technology.

Description

bPOL48V is a buck DCDC converter. The main advantages of this topology are its simplicity and low number of active devices. However, the current in the power switches may have fast current rise and fall times, which increase the voltage stress if the switching speed and Printed Circuit Board (PCB) are not carefully optimized.

Furthermore, the switching frequency fs selection is critical to find the optimal trade-off between size of the main inductor, output filter requirements and efficiency.

Due to the magnetic field of up to 4 Tesla present in the environment, the use of magnetic cores for the inductor is not possible. In this condition, the switching frequency should be increased as much as possible in order to reduce the size of the inductor. Therefore, GaN power devices constitute a very attractive alternative, given their excellent switching performance and inherent radiation tolerance.

bPOL48V converter is based on the EPC2152 GaN power stage, which is able to provide the required 10A current at maximum 80V input voltage, which gives enough room to operate reliably at 48V dc input voltage. Additionally, this device integrates the driving stage as well as the level shifters and boostrap capacitor charging circuit. The monolithic integration and the LGA chip scale package allow to reduce the driving loop impedance, and to optimize the power loop impedance by means of the careful design of the PCB.

The controller (GaN_Controller) has been designed at CERN using the I3T80 onsemi high-voltage 0.35µm CMOS technology. Among the main features of this controller, it should be highlighted the radiation tolerance, the integration of all the regulators and voltage references required for the control circuitry, the voltage-mode control, the real-time optimization of dead time between the PWM driving signals, and the adjustable switching frequency.

GaN_Controlelr and EPC2152 are indicated on the board picture in Figure 1.

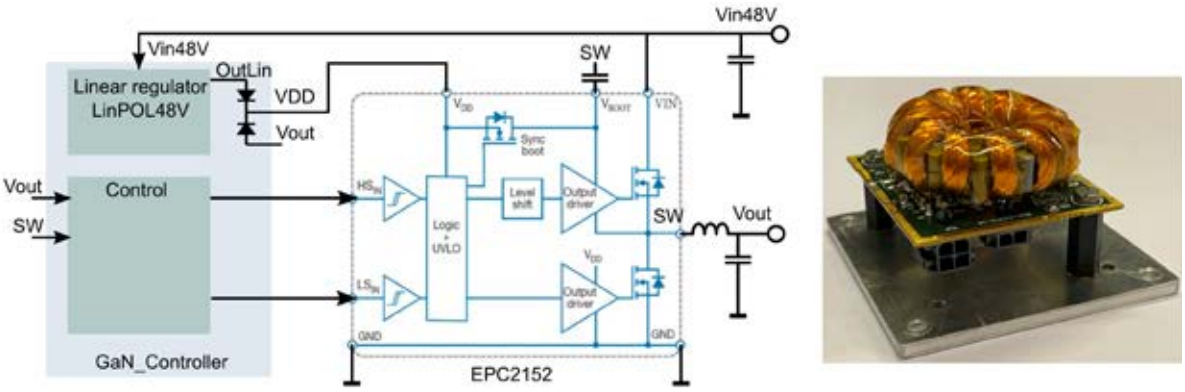


Fig.2: bPOL48V block diagram (left) and photo of the PCB (right).

Figure 2 shows the block diagram of bPOL48V (left) and the picture of the test PCB (right). The converter size is 43mmx49mm and the thickness including the inductor and power connectors is 27mm. The PCB has been optimized to minimize the parasitic inductance of the input loop, to avoid overvoltage spikes. Furthermore, to increase efficiency, the controller internal linear regulator is used only for startup. When the converter reaches V_{out}=12V, the internal diode between $OutL_{in}$ and VDD becomes reverse biased, and the circuit logic is supplied from V_{out}.

Results

The tests performed on the bPOL48V include the switching performance, the efficiency and the radiation tolerance.
In order to evaluate the switching performance, the switch node voltage (SW in the Figure2) has been measured. The voltage overshoot in this node, representative of the power loop impedance, should be kept below the maximum value of the GaN power devices (80V). In this case, the measured peak voltage is 63V for V_{in}= 48V and 10A load, which is within the safe operating area. Furthermore, a damped ringing with 3ns period and 10ns duration was observed, which agrees with the parasitic inductance obtained using finite elements simulations during the design phase.

The efficiency of the converter, shown in the Figure 3, was evaluated using the custom air-core inductor shown in the Figure 1 and 2MHz switching frequency, for different input voltages and up to 10A load. It should be noted that, due to the large current ripple amplitude, the converter operates with negative switching-on current (indicated by the circular markers in the efficiency curves) or hard switching (star markers), depending on the load and input voltage conditions. The measured efficiency at maximum load and input voltage is above 92.5%.

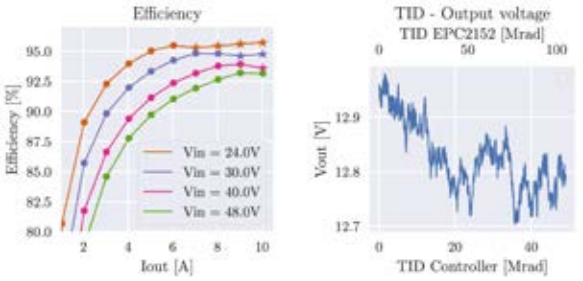


Fig.3: bPOL48V efficiency (fs=2 MHz) (left), TID (right).

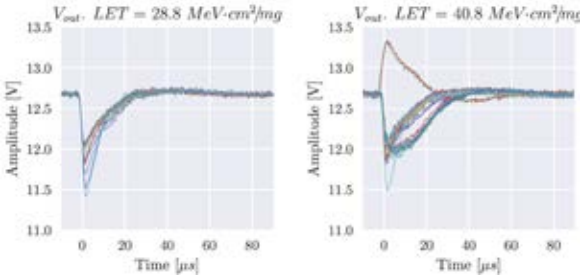


Fig.4: bPOL48V Single event transients.

In order to assess the radiation tolerance, the Total Ionising Dose (TID), Single Event Effects (SEE) and Displacement Damage (DD) have been evaluated.

To study the TID effects, the converter was irradiated using the X-ray Seifert RP149 irradiation system, part of the CERN-EP-ESE equipment. As shown in the Figure 3, adjusting for the difference in position and material, the reached TID is 50 MRad (first 10 MRad at 0.4 MRad/h and the remaining at 2.16 MRad/h) for the controller (Si), and 128 MRad (first 20 MRad at 0.9 MRad/h and the remaining at 4.6 MRad/h) for the power devices (GaN). As it can be seen, there is no appreciable change in the performance. Efficiency and internal regulators were also monitored during irradiation, where no degradation was detected.

The controller has been tested for SEE in the Cyclotron Resource Center at UCLouvain. In this test, the GaN power devices are not affected due to the thickness of the package. The converter was irradiated with heavy ions at LET=28.8 MeV·cm^2/mg and LET=40.8 MeV·cm^2/mg, reaching 5e^6 ions in both cases. The acquired events are shown on Figure 4, where 19 transients are observed for the lower LET and 31 events for the larger one, with amplitude within pm 10% and duration between 20mu s and 40mu s. Furthermore, no resets or destructive events were detected. For the GaN power devices, independent tests have been conducted by the manufacturer, showing SEE tolerance for linear energy transfer exceeding 84MeV cm^2/mg.

Finally, the controller was tested for DD using proton and neutrons irradiation.
The protons irradiation was performed in the MC40 Cyclotron Facility in Birmingham, using a 25MeV beam. No effects were observed for fluences up to 2.23e^{14} p/cm^2. However, at 3.3 e^{14}p/cm^2 and 5e^{14} p/cm^2 the converter was functional but with oscillations in one of the internal regulators.
The neutrons irradiation was performed in the TRIGA reactor, in Ljubljana. The converter was fully functional for fluences up to 4e^{14} n/cm^2, but failed to start when irradiated above 7e^{14} n/cm^2. The failures are most probably in the high voltage vertical transistors used in the controller internal linear regulator. Similarly as for the SEE, the manufacturer of the GaN power devices measured the DD using neutron irradiation up to 1e^{15} n/cm^2, without observing any significant degradation.
(For EPC2152 radiation tests please refer to: L. Max Zafrani, “Radiation Performance of Enhancement-Mode Gallium Nitride Power Devices”).

Why EUROPRACTICE?

We used EUROPRACTICE Sevices because it has been the only way for us to access this technology, to participate to the MPW runs and to go for production in a MLM engineering run for 30 wafers.

Acknowledgements

This work has been carried out thanks to the CERN EP WP5.2 R&D program and the CERN KT funds.

3.1-51GHz Ultra-widely tunable, low-power LC oscillator for RF and mmW frequencies

Cornell University, USA

Contact: Thomas Tapen
E-mail: tpt26@cornell.edu
Technology: ST 28nm FD-DSOI CMOS
Die size: 2mm x 1mm
Application Area: Education

Introduction

The expansion of wireless communication and sensing frequency bands both at traditional RF frequencies and now at mmW frequencies. Rather than addressing multi-band operation by having multiple different RF front-ends, unified, tunable front end components would be preferred, however this can be quite difficult. While existing software-defined radio (SDR) hardware exists for sub-6GHz bands, this work focuses on extending wideband/widely-tunable SDR techniques to mmW frequencies.

Description

The design and its measured results are fully given in [1], and summarized below.
We have designed an ultra-widely tunable, low-power LC oscillator suitable for LO synthesis from traditional microwave frequencies up to and beyond 5G mmW bands. This record 3.1-51GHz tuning range is enabled by a novel lumped/distributed LC resonant circuit, the compact tunable transmission line (CTTL).

Results

The VCO achieves a continuous tuning range of 3.1-51GHz, a record for single-ore LC oscillators. The VOC also achieves record tuning figure of merit (FOMT) for multi-octave tunable oscillators with mmW frequency outputs. It is also the only design (to our knowledge) that outputs mmW frequencies as well as sub 6-GHz frequencies without the use of frequency dividers which, allows for very low (<8mW, <2mW @ 3.1GHz) power consumption and good FOMT.
Therefore, the presented VCO represents one of very few CMOS integrated oscillator designs that can operate both at 5G mmW frequqncies between 20 & 40GHz, while also supporting more traditional frequencies. This is achieved

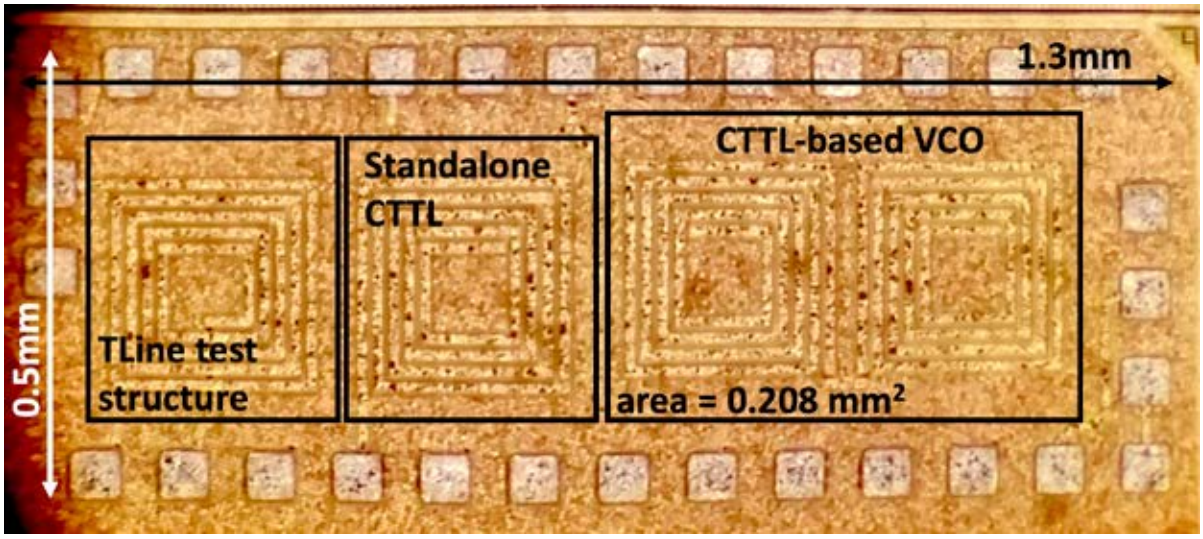


Fig.1: The manufactured die including the VCO and test structures.

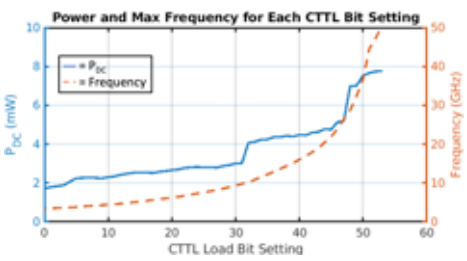


Fig.2: Power consumption and oscillation frequency as a function of valid CTTL switch states.

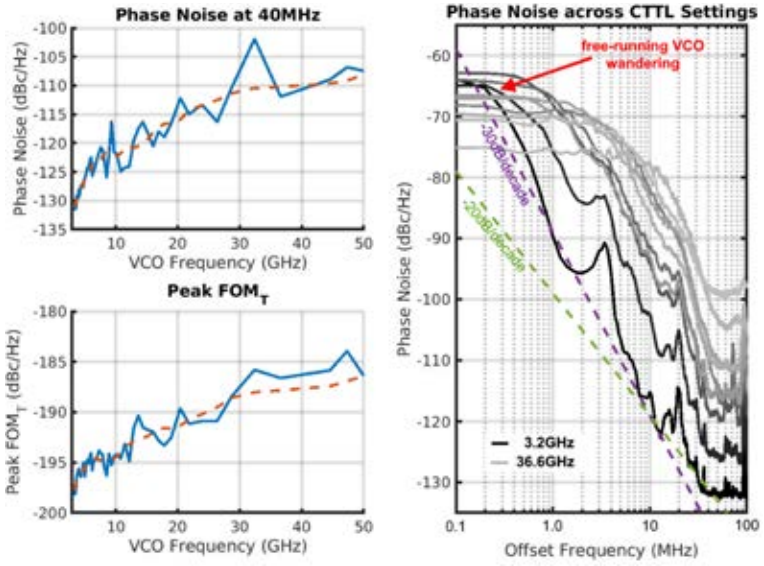


Fig.3: Phase noise and FOMT across tuning, plus representative SSB phase noise plots for different output frequencies.

with low power consumption, compact area (0.208mm^2 oscillator core area), and in an un-modified (i.e. non-MEMs) CMOS technology.

Why EUROPRACTICE?

This work was supported by STMicroelectornics in their 28FDSOI technology, and the CTTL design benefits greatly from SOI technologies. CMP provides MPW runs in this technology for this kind of prototyping work.

Acknowledgements

This work was supported by a silicon donation by STMicroelectronics, and test equipment provided by the Cornell Center for Materials Research (CCMR) under NSF award DMR-1719875.

References

[1] T. Tapen, A. Cathelin, and A. Apsel, "A 3.1-51GHz, Sub-8mW, Single-Core LC VCO Based on a Novel Compact Tunable Transmisison Line (CTTL) Resonator in 28nm FDSOI CMOS," 2021 IEEE Radio Frequency Integrated Circuits Conference (RFIC), 2021. Pp. 191-194, doi: 10.1109/RFIC51843.2021.9490503.

5.5 GHz phase-mux-based O-QPSK transmitter for image applications

Institute of Electrical and Optical Communications Engineering, University of Stuttgart, Germany

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E-mail:	sefa.oezbek@int.uni-stuttgart.de
Technology:	ST 130nm BiCMOS9MW
Die size:	2.4mm x 1.3mm incl. seal ring
Design Tools:	Cadence Virtuoso
Application Area:	IoT

Introduction

In this proposed work, we develop a 5.5 GHz phase-mux-based Offset Quadrature Phase Shift Keying (O-QPSK) transmitter for image applications with digital video interfaces up to 16 - bit (at a total data rate of ~ 171.8 Mbps) by using ST 130nm BiCMOS9MW. O-QPSK transmitter structure is implemented to reduce the number of RF building blocks and consequently the power consumption. Thus, it allows the system to be used in mobile biomedical applications as well.

Description

The O-QPSK modulation signal is generated by using an IQ divider by two. One of the four quadrature phases is then selected according to the 2-bit baseband data via the 4x1 NAND-MUX. In combination with a class-D-1 power amplifier (PA), a fully integrated O-QPSK transmitter is realized.

By limiting the phase shift to no more than 90° at a time, lower amplitude fluctuations occur, thus the linearity requirement of the PA is relaxed. The whole chip, including the on-chip transformer, occupies 2.4 mm x 1.3 mm, including a seal ring.

Results

The simulated total power consumption of the O-QPSK modulation circuit in 130nm CMOS draws about 77 mA from a 1.2 V supply, while the PA stand-alone dissipates 58 mA at 0.55 V supply. According to the post-layout simulation results, the current mode (inverse) Class-D power amplifier delivers an output power of about 9 dBm at 5.5 GHz.

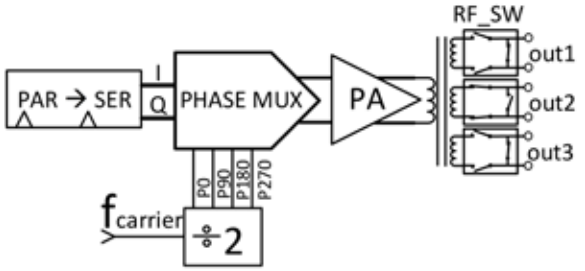

Fig.1: Block diagram of O-QPSK.

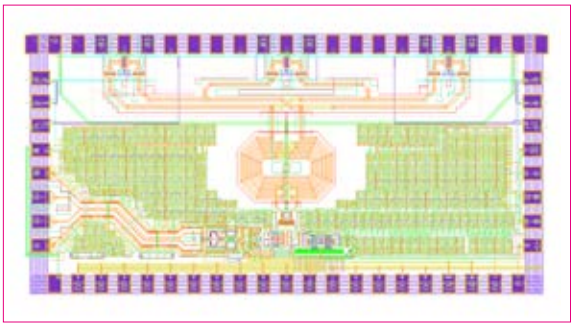

Fig.2: Layout of O-QPSK transmitter.

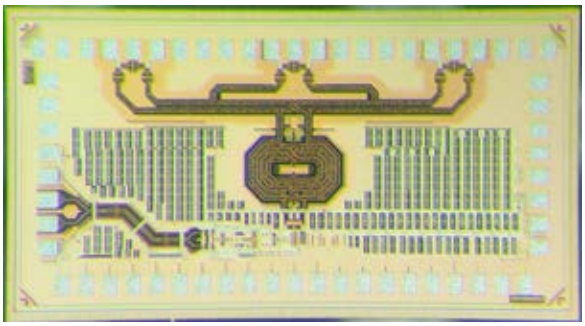

Fig.3: Photograph of O-QPSK transmitter IC.

Why EUROPRACTICE?

CMP / EUROPRACTICE offer prototype services and testing for state-of-the-art technologies with mature PDKs at reasonable prices. Without these services we as a University could not participate in such design-centric projects. They also provide excellent support for PDKs and tape-out procedures till the GDS submission.

Acknowledgements

This project is supported by Deutsche Forschungsgemeinschaft (DFG) through the FFlexCom-Project Project number 255449811.

References

https://www.int.uni-stuttgart.de/en/research/ic/fflexcom

NMR-Needle: co-integration of a miniaturized Magnetic Resonance (MR) detection coil with the complete MR transceiver on a single implantable sensor

University of Stuttgart, Institute of Smart Sensors, Stuttgart, Germany

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E-mail:	frederik.dreyer@iis.uni-stuttgart.de
Technology:	ST 130nm BiCMOS9MW
Die size:	5mm x 0.4mm
Design Tools:	Cadence Virtuoso
Application Area:	Medical / Health

Introduction

The presented chip was designed to conduct in-vivo magnetic resonance (MR) experiments inside rat brains. By co-integrating a miniaturized MR detection coil with the complete MR transceiver on a single implantable sensor, this so-called NMR-on-a-chip approach [1] offers greatly superior sensitivity and signal robustness compared to extracorporeal detection coils and passive implantable MR coils [2]. The presented chip is the next generation of the device presented in [2], further improving its performance and application range in the target MR application as well as minimizing tissue damage during the implantation surgery by using an optimized chip geometry. Applications of the presented device include, e.g., the detection of changes in blood flow and oxygenation [2] as well as in-vivo MR imaging and heteronuclear MR spectroscopy.

Description

The presented MR ASIC co-integrates a miniaturized MR detection coil with an RF transceiver circuit, including the required frequency generation module, cf. Figure 1. The transmitter uses an H-bridge power amplifier (PA) to produce the elevated output currents necessary to excite the nuclear spins. The receiver path amplifies and conditions the spin-related MR signal picked up by the detection coil. It consists of a low noise amplifier (LNA), followed by a quadrature downconversion mixer and a variable gain amplifier (VGA) output stage with a large driving strength to drive the pads and the long cable connecting the implanted device with the extracorporeal ADC and digital signal processing unit. The frequency generation module produces the LO signal that is used to drive both the PA as well as the downconversion mixers. It features a second order integer-N phase-locked-loop (PLL) with a programmable frequency multiplication factor ranging from 1 to 64.

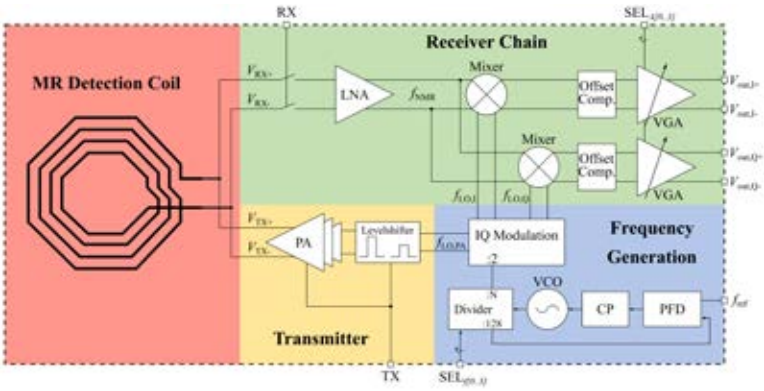

Fig.1: Block diagram of the ASIC.

The on-chip MR coil is implemented in the two thick top metal layers provided by ST's BiCMOS9MW technology. By connecting multi-turn coils in the two layers in series, the induced MR signal can be maximized to alleviate the burden on the receiver electronics.

To allow for an implantation with minimum tissue damage, the dies are post-processed by mechanically thinning them down to 80µm and producing a tip at an optimized angle by wafer dicing, cf. Figure 2.

Results

The functionality of the chips was first verified by performing a complete electrical characterization of the transceiver electronics. To measure the conversion gain of the LNA and the mixers, a low-power signal was inductively coupled into the on-chip coil. In this way, a conversion gain of up to 36 dB was measured. Based on this gain measurement, the input-referred noise of the LNA was determined. Over the whole frequency range of interest (40 MHz up to 600 MHz) the input noise is lower than 700 pV/√(Hz), with a minimum value of 300 pV/√(Hz) at 600 MHz, due to the parasitic tuning of the MR coil by the LNA input capacitance, cf. Fig. 3. The maximum output current of the PA is 200 mA.

The ASICs are currently tested in in-vitro and in-vivo measurements in a 14.1 T small animal MR imaging scanner by our partners at the Max Planck Institute for Biological Cybernetics in Tübingen.

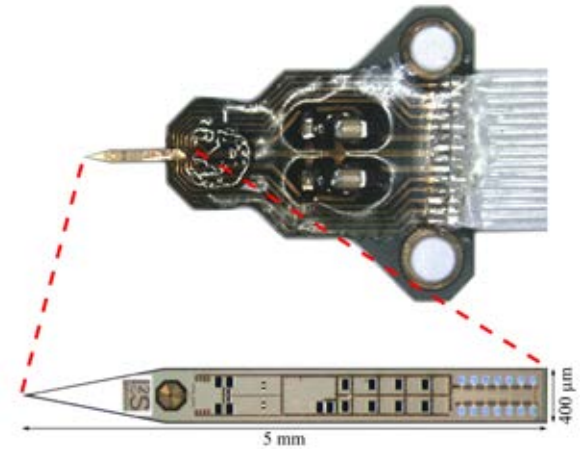

Fig.2: Micrograph of the post-processed die.

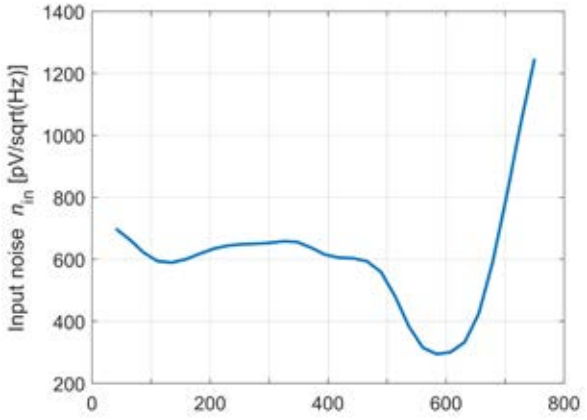

Fig.3: Input referred noise of the NMR receiver as a function over frequency.

Why EUROPRACTICE?

We selected the STMicroelectronics BiCMOS9MW technology due to its combination of a high-performance analog CMOS process with high-performance n-channel BJTs that we use for the high-performance broadband LNA.

Our experiences with CMP's technical support team are excellent. They are constantly exceeding our expectations with a very fast response time to solve any technical problem even shortly before tapeout dates. Moreover, the prices offered by CMP for design tools and manufacturing are very attractive and represent a key enabler for research institutes to be able to stay in the IC design business.

References

[1] J. Anders, F. Dreyer and D. Krüger, "On-Chip Nuclear Magnetic Resonance," in Handbook of Biochips: Integrated Circuits amd Systems for Biology and Medicine, Springer New York, 2020, pp. 1-32

[2] J. Handwerker et al. "A CMOS NMR needle for probing brain physiology with high spatial and temporal resolution" Nature Methods 17.1 (2020), pp. 64-67

A 67mW D-band FMCW I/Q Radar Receiver with an N-path Spillover Notch Filter in 28nm CMOS

Vrije Universiteit Brussel (VUB), Belgium
imec, Leuven, Belgium

Contacts: Anirudh Kankuppe, Sehoon Park, Kristof Vaesen, Dae-Woong Park, Barend Van Leimpd, Siddhartha Sinha, Piet Wambacq, Jan Craninckx
E-mail: anirudh.kankuppe@imec.be
Technology: TSMC 28nm HPC+
Die size: 2.4mm x 1.2mm
Application Area: IoT

Introduction

For the complex operations like gesture recognition and imaging, large RF bandwidth hence small range resolution is desired. In D-band (110-170Ghz) where large bandwidth is available, the system can be scaled down and compact arrays are possible. In such a scenario, the resilience of the receiver to the TX-to-RX leakage termed as spillover is crucial. The designed receiver addressing the above problems, is suitable for a high resolution imaging radar for its high RF bandwidth or for an automotive radar where high spillover resilience is desired and selective target attenuation can be employed.

Description

The receiver front-end consists of an on-chip antenna and LNA with broadband interstage matching transformers and passive I/Q mixers. The LO is generated with an on-chip, Branchline coupler (BLC) based chain. The baseband contains an N-path filter capable of narrowband attenuation. The filter frequency is adaptable and the attenuation can be extended to the nearby large targets thus making the receiver resilient to the reflections along with the spillover.

Results

The receiver is characterized with 53dB of conversion gain with 18GHz of RF bandwidth with 8dB NF (5.6dB EINF) (Figure 2). A constant 26dB spillover attenuation over the RF bandwidth is measured (Figure 3) and the selective nearby target attenuation of 19dB is demonstrated. A range resolution of 1.3cm is also measured with verified range and doppler functionality. The total system power is 67mW.

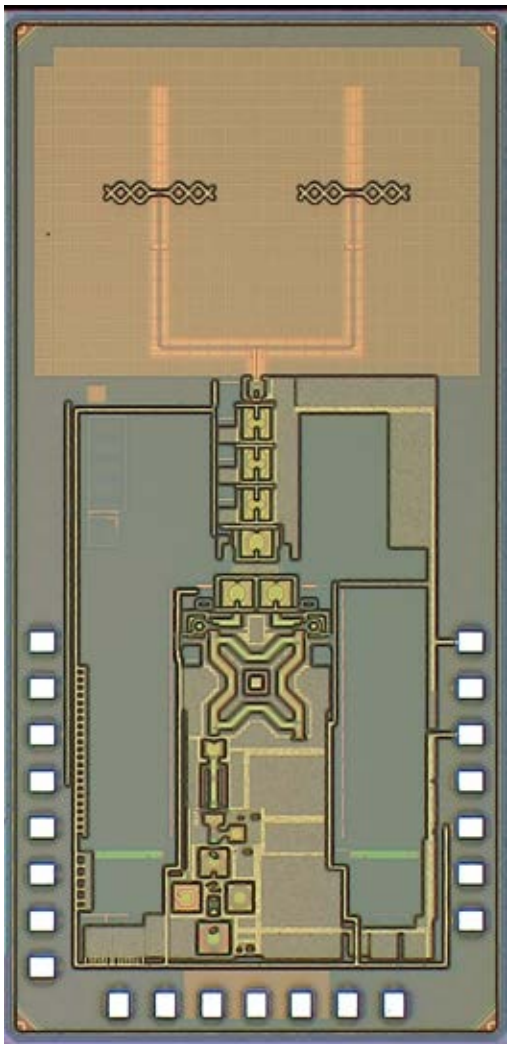

Fig.1: Designed receiver in 28nm CMOS (dimensions: 1.2mm X 2.4mm).

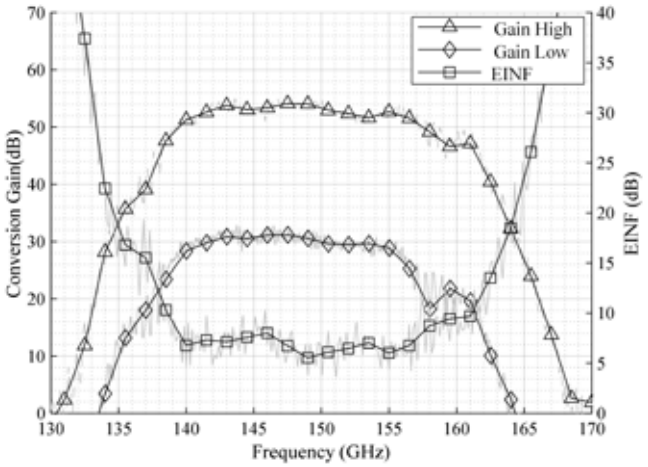

Fig.2: The Conversion Gain and the EINF of the receiver.

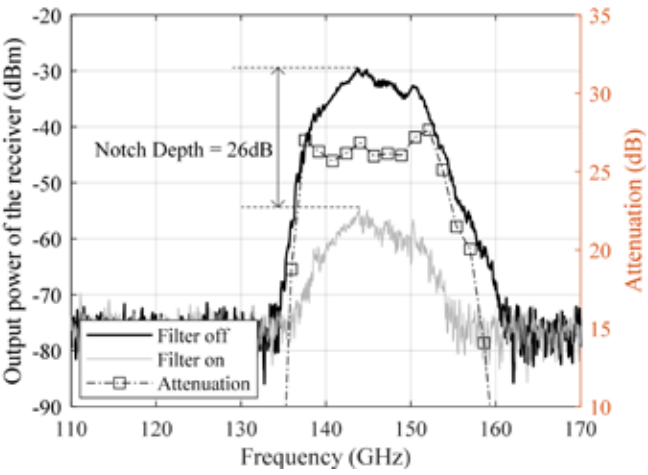

Fig.3: Receiver output showing spillover attenuation.

The work stands among the state-of-the-art D-band receivers in terms of low-power, high RF bandwidth and a unique narrow band spillover attenuation capability.

Why EUROPRACTICE?

Imec's partnership with EUROPRACTICE has seen many state-of-the art designs in the past. The collaboration provides a unique opportunity to test our research in advanced nodes in a cost-effective manner. The experience with EUROPRACTICE was always smooth in terms of GDS handover and the support in terms of the tools/licenses needed for the research.

Acknowledgements

The research leading to these results has received funding from the European Community's ECSEL Joint Undertaking under grant agreement n° 783190 - project PRYSTINE.

References

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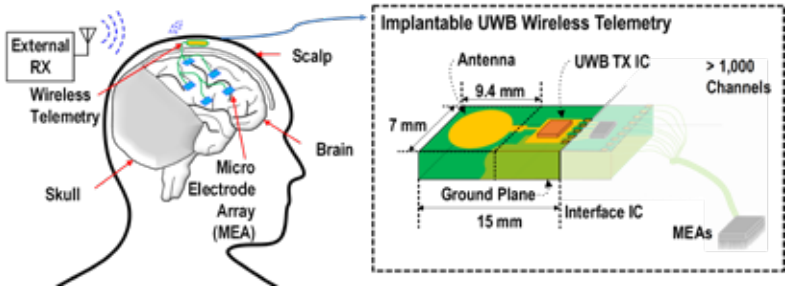

Fig.1: Implantable Wireless Telemetry.

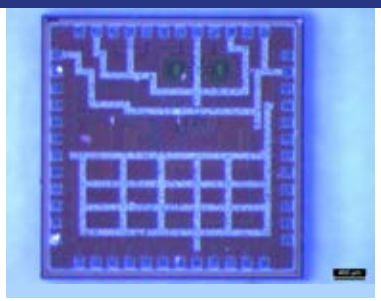

Fig.2: Photo of the implantable high-speed IR-UWB transmitter ASIC in 28nm CMOS..

High data rate and energy efficient IR-UWB transmitter for implantable brain-computer interfaces

imec Netherlands, Eindhoven, the Netherlands

Contacts: Minyoung Song, Yao-Hong Liu
E-mail: yao-hong.liu@imec.nl

Technology: TSMC 28nm HPC+
Die size: 1.3µm x1.3µm
Design Tools: Cadence
Application Area: Medical / Health

Introduction

Intra-cortical extracellular neural sensing is being rapidly and widely applied in several clinical research and brain-computer interfaces (BCIs), as the number of sensing channels continues to double every 6 years.

Since each neural sensing channel typically samples at 20 - 50kSps with a >10b ADC, multiple MEAs demand a data transfer rate up to Gbps.[2] However, these BCIs are severely hindered in many clinical uses due to the lack of a high-data-rate and miniature wireless telemetry solution that can be implanted below the scalp, i.e., transcutaneously.

The area of the wireless telemetry module should be miniaturized to ~3cm^2 due to anatomical and neurosurgical implantation constraints. The transmission range up to 10cm is highly desirable, in order to improve the reliability of the wireless link against e.g. antenna misalignment, etc.

We aim to develop a high data rate, miniature and implantable wireless transmitter that can cover up to 10 cm of transmission distance.

Description

In this work, instead of increasing modulation order (bits per symbol), we use a hybrid impulse modulation that employs an agile digital polar-based IR-UWB TX to combine 4PAM, 8PSK, and 4PPM. A digital polar IR-UWB transmitter that has asynchronous pulse shaping is designed. We also present a power-efficient delay generator for a calibration-free M-PPM and a low-noise 8-phase ring oscillator with duty-cycle correction for an accurate M-PSK.

Results

The UWB TX IC was occupying the core area of only 0.155mm^2. The wireless module implemented on an FR4 PCB has a core electronic area of only 1.05cm^2, including the TX IC and a printed circular monopole antenna. The measured transmission ranges are 2 and 15cm at 1.66 and 1.43Gbps data rates.

The table below summarizes the performance and benchmarks with state-ot-the-art transcutaneous and high data rate UWB TXs.

	This work	[4]	Ando, TBioCAS'16	[2]	[3]	[5]
Device technology	28nm CMOS	180nm CMOS	GaAs HBT	VCSEL	65nm CMOS	28nm CMOS
Wireless method	IR-UWB	IR-UWB	IR-UWB	Optical	IR-UWB	IR-UWB
Frequency	6-9GHz	3-7GHz	8GHz	NIR	4GHz	3-10GHz
Modulation	4PPM+BPSK+ 4PAM impulse	BPSK impulse	OOK impulse	OOK impulse	D-MPPM impulse	BPSK impulse
TX architecture	Digital polar (DPA+ PHMUX)	Edge combine	Edge combine	-	Edge combine	Digital polar (DPA+ ILRO)
Max. data rate	**1.66Gbps**	500Mbps	128Mbps	300Mbps	1.125Gbps	27Mbps
TX power cons.	9.69mW	5.4mW	561mW	11mW	28mW	4.9mW
TX energy efficiency	**5.8pJ/b**	10.8pJ/b	438pJ/b	37pJ/b	25pJ/b	180pJ/b
Tissue thickness	15mm skin/fat	2mm skin/fat & 4mm bone	15-20mm phantom	3.5mm skin	No tissue	No tissue
Transmission range (in-vitro)	**2cm**@1.66Gbps **15cm**@1.43Gbps	1.5cm	1cm	0.4cm	N.A.**	-**
Normalized energy eff.*	**45pJ/b/m** (@1.43Gbps)	720pJ/b/m	43.8nJ/b/m	9.25nJ/b/m	-	-

*TX energy efficiency normalized to 1m transmission range. ** No transmission range reported with tissue or phantom.

Why EUROPRACTICE?

EUROPRACTICE provides unique mini@sic service for the research organizations in Europe to access the technology from the world-leading foundries, like TSMC, so we can develop the research ASIC prototype. The PDK and design integration services are also very good.

References

[1] M. Song et al., "A 1.66Gb/s and 5.8pJ/b Transcutaneous IR-UWB Telemetry System with Hybrid Impulse Modulation for Intracortical Brain-Computer Interfaces, " ISSCC, Feb. 2022.

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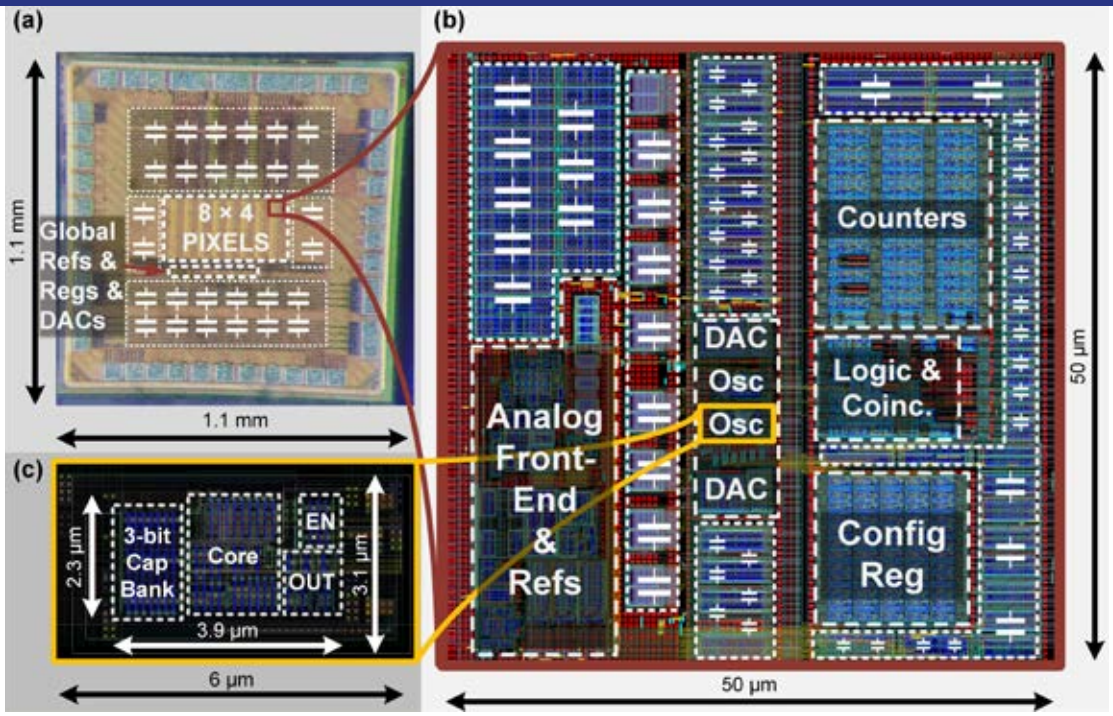

Fig.1: Readout IC prototype for X-ray hybrid pixel detectors: (a) chip photograph, (b) layout of the pixel and (c) layout of the ring oscillator.

Vernier based Time to Digital Multichannel Converter in TSMC 28nm Process

AGH University of Science and Technology, Krakow, Poland

Contacts: Lukasz Kadlubowski, Piotr Kmon
E-mails: lukasz.kadlubowski@agh.edu.pl, piotr.kmon@agh.edu.pl

Technology: TSMC 28nm HPC
Die size: 1.120mm × 1.120mm
Design Tools: Cadence Virtuoso, Spectre, Xcelium; Siemens Calibre
Application Area: High Energy Physics (HEP)

Introduction

The design prototype is a readout IC for hybrid pixel detectors. It addresses the need to measure time of arrival (ToA) of X-ray particles with high resolution and indirectly measure energy of each particle using time over threshold (ToT) method. This functionality is essential in 3-D particle tracking and is used in electron microscopy and antimatter research. Our aim is to achieve the resolution on the order of tens of picoseconds.

Description

The chip prototype consists of 8×4-pixel matrix with 50µm pitch and a global part. Each pixel has a functionality of ToA/ToT measurement or, alternatively, single photon counting (SPC). The pixel consists of an analog front-end and a digital part with time-to-digital converter (TDC). The analog front-end consists of an amplifier, a discriminator, supported by a calibration block and a threshold setting block. The digital part of the pixel includes Vernier TDC with two ring oscillators and their calibration circuits, as well as counters/shift registers. The pixel is highly configurable with in-pixel configuration bits. SPC/ToT counter depth is 13-bits, ToA counter depths are 13-bit and 9-bit for a coarse counter and a fine counter, respectively. ToA range and resolution depends on the frequency of the oscillators, which is on the order of 1-4 GHz.

Why EUROPRACTICE?

AGH University benefits from the EUROPRACTICE offer since many years, with a lot of successful tapeouts. EUROPRACTICE offers affordable fabrication of our prototypes in MPWs and mini@sics and provides access to a wide variety of design tools. It is an essential partner in our research.

Acknowledgements

The presented work has been supported by the National Science Center, Poland under Contract No. UMO-2016/23/D/ST7/00488.

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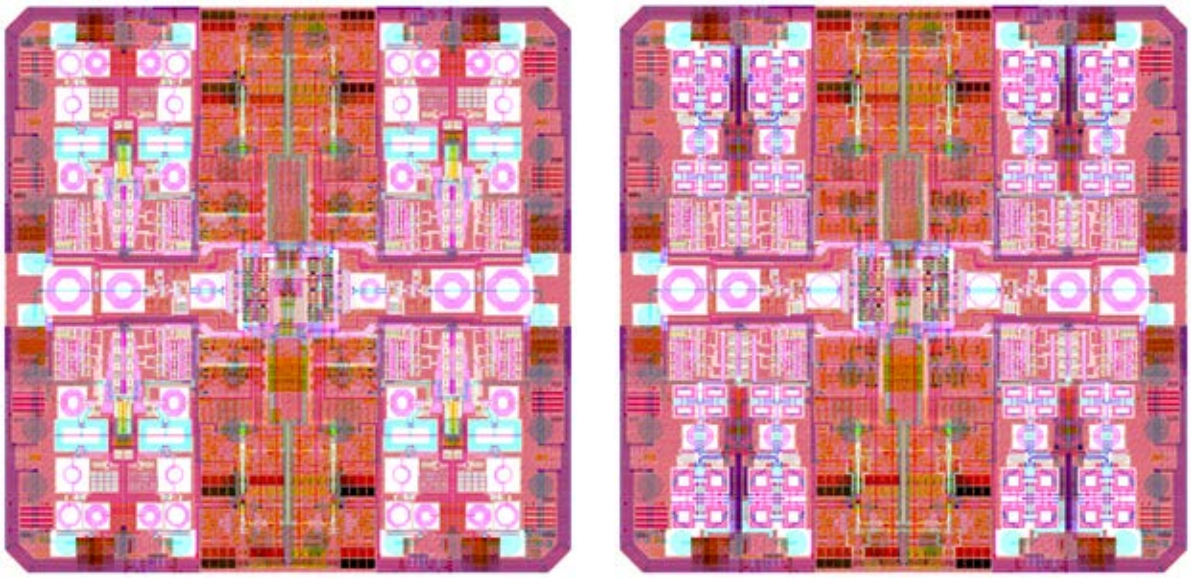

Fig.1: Top-Level Layout of TRV003TSM40LP (left) and TRV004TSM40LP (right).

The KuKa Project – Quad-Rx-Path and Quad Tx-Path Dual-Beam Dual-Polarisation Ku-Band Phased-Array RFICs for Low-Cost LEOSAT Electronically-Steerable Antennas

Tetrivis LTD, Basingstoke, United Kingdom

Contact: Jide Adeniran
E-mail: jide@tetrivis.com
Technology: TSMC 40nm CMOS LP
Die size: 2 times 1.728mm x 1.728mm
Application Area: (Aero)Space

Introduction

TRV003TSM40LP (Receive) and TRV004TSM40LP (Transmit) Phased-Array RFICs are products in Tetrivis' KuKa mm-Wave/RFIC portfolio targeted at Electronically-Steered Antennas (ESA) for the Satellite-Communication market. Ku-Band (10GHz to 15GHz) is used predominantly in Europe and in the Americas. Ka-Band (17GHz to 30GHz) is used predominantly in Asia and China.

As the likes of Space-X (Star-Link project), Amazon (Kuiper project), Leosat, OneWeb and a few other corporate and national entrants into the emerging LEO-SAT market, continue global LEO-SAT constellations deployment, the entire 7 billion people in the world will have high-speed access to the Internet via LEO-SATs by 2030. But they will need very low-cost ESAs to take advantage of this unprecedented access. There is currently no Phased-Array Rx or Tx RFICs in the market that can simultaneously achieve Ka-Band and Ku-Band operability.

We set ourselves a challenge to implement Rx and Tx RFICs that can be used in Ku- and Ka- Bands without compromising Transmit Output Power and Receive Noise Figure performance.

Such Rx and Tx RFICs will greatly lower ESA bill-of-materials, enable companies to develop ESAs with global interoperation capability and make the LEO-SAT ESAs truly low-cost and affordable to the Third World.

Description

TRV003TSM40LP employs direct-down-conversion architecture and contains four Dual-Beam and Dual-Polarisation Ku-Band Receive paths.

TRV004TSM40LP employs direct-up-conversion architecture and contains four Dual-Beam and Dual-Polarisation Ku-Band Transmit paths.

Both RFICs have limited conceptual support for Ka-Band frequencies. Analogue Beam-Forming is carried out at Baseband Frequencies. All KuKa RFICs in a Phased-Array ESA implementation are addressed using the same serial clock and data interface with the available address space enabling a Dual-Beam Dual-Polarisation Phased-Array Receiver or Transmitter ESA product with up to 1024 TRV003TSM40LP RFICs (Rx), up to 1024 TRV004TSM40LP RFICs (Tx), up to 4096 antenna elements and up to 36dB antenna gain.

Why EUROPRACTICE?

EUROPRACTICE has always provided access to advanced cutting-edge fabrication technologies at a good price for small companies, research institutes and academia. Without EUROPRACTICE, access to these technologies for small companies will be next to impossible. The support EUROPRACTICE provided at pre-design, design, post-design, fabrication and post-fabrication phases of the project was outstanding.

Supply Insensitive DPLL

Delft University of Technology, The Netherlands

Contact: Yue Chen
E-mail: Y.Chen-1@tudelft.nl

Technology: TSMC 40nm CMOS LP
Die size: 1100µm x 1880µm
Design Tools: Cadence. Synopsys Design Compiler and IC Compiler
Application Area: IoT

Introduction

Integrated circuits and systems are generally powered by switch-mode DC–DC converters, which transforms the voltage level of an energy source into the system's nominal supply voltage with sufficiently high efficiency. However, if the DC–DC converter directly supplies sensitive analog or RF circuits, such as oscillators and phase-locked loops (PLLs), its output ripples could severely degrade their performance. Consequently, a low dropout (LDO) linear regulator is typically inserted after the switching converter to suppress the ripples. However, the LDO may require external components and/or lead to relatively high power overhead, impacting the system power efficiency. Moreover, to isolate the sensitive oscillator from the clocked phase detection circuitry, PLLs usually require two separate LDOs, thereby worsening the system complexity and cost. Consequently, it deems beneficial if the PLL could be powered directly from the DC–DC converter, thus entirely avoiding the LDOs.

Description

In this project, we designed a 4.5–5.1-GHz fractional-N digitally intensive phase-locked loop (DPLL) capable of maintaining its performance in face of a large supply ripple, thus enabling a direct connection to a switched-mode DC–DC converter. Supply pushing of its inductor-capacitor (LC) oscillator is suppressed by properly replicating the supply ripple onto the gate of its tail current transistor, while the optimum replication gain is determined by an on-chip calibration loop that is also tolerant of supply variations.

A proposed configuration of cascading a supply-insensitive slope generator with an output of a current digital-to-analog converter (DAC) linearly converts the phase error timing into a corresponding voltage, which is then quantized by a successive approximation register (SAR) analog-to-digital converter (ADC) to generate a digital phase error. We also introduce a low-power ripple pattern estimation and cancellation algorithm to remove the phase error component due to the supply-induced delay variations of loop components.

Results

The DPLL is powered by a 1.0-V supply, the whole loop consumes 3.25mW (1.02mW for DCO, 0.92mW for PD, and 0.63mW for the digital part). Using 50MHz reference, the DPLL prototype achieves the performance of 428-fs rms jitter, <–55-dBc fractional spur, and <–54-dBc maximum spur while consuming 3.25mW and being subjugated to a sinusoidal or sawtooth supply ripple of 50 mVppat 50-MHz reference divided by 3, 6, or 12.

Why EUROPRACTICE?

We have taped-out through EUROPRACTICE for several times. EUROPRACTICE has provided us an easy way to tape-out our design with the technology we prefer.

Acknowledgements

We would like to tank Zhong Gao from the Delft University of Technology and Yao-Hong Liu and Johan Dijkhuis from the imec-nl Holst Center for technical discussion and assistance. They would also like to thank Atef Akhnoukh and Zu Yao Chang for their help with the tape-out and chip bonding.

References

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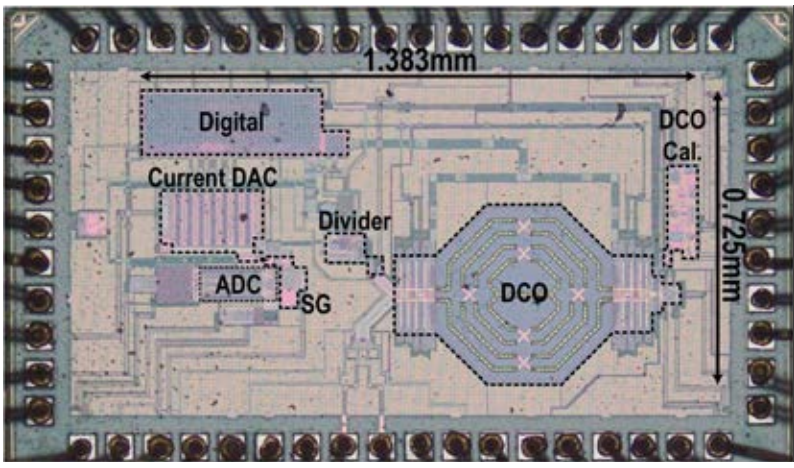

Fig.1: Chip micrograph of the DPLL.

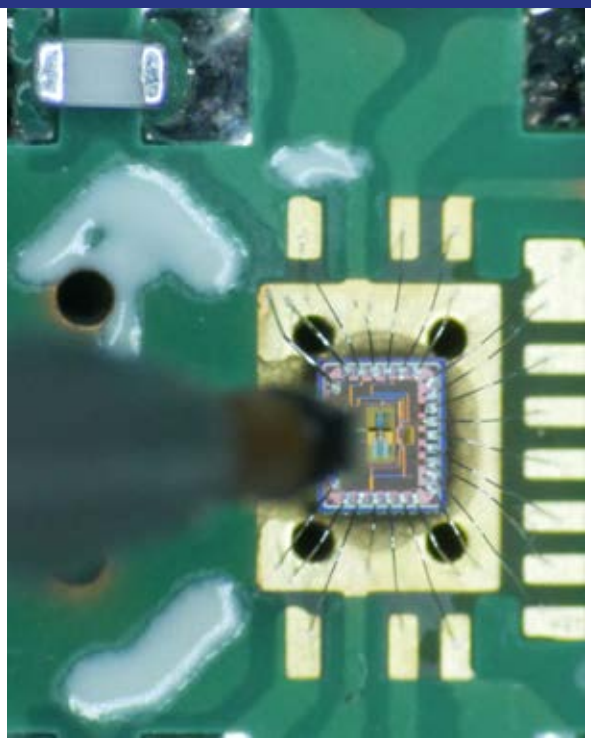

Fig.1: The photo of the chip on the PCB board.

Three-Winding Transformer-Based mm-Wave Fundamental Frequency Oscillator

Eindhoven University of Technology, The Netherlands

Contacts:	Dr. ir. Hao Gao, Dr. Yun Fang
E-mail:	h.gao@tue.nl
Technology:	40nm CMOS LP
Die size:	1.850µm x 1.850µm
Design Tools:	Cadence
Application Area:	Datacom / Telecom

Introduction

Typical applications in the 60 GHz ISM band, such as wireless high-definition video streaming, require a quality reference signal to avoid receiver sensitivity degradation and improve transmitter signal quality. IEEE 802.11.ad is a high-data-rate communication standard using a 60 GHz band. It could provide at least 2 Gbit/s data rate within the range of 10 m. IEEE 802.11. ad supports new multimedia applications such as in-door VR and WPAN, extending the 5G communication for indoor applications with this data rate. However, complex modulation and coding schemes employed there require low distortion, leading to strict specifications on a transmit (TX) error vector magnitude (EVM). For example, the IEEE 802.11ad standard requires a TX EVM of −21 dB for a 16 QAM modulation [1], which sets stringent phase noise (PN) requirements on the local oscillators (LOs) [2]. A wide tuning range (TR) is also necessary to cover the specified frequency bands (e.g., 57–65 GHz) with margins for process and temperature spreads. Meanwhile, a long battery lifetime calls for high power efficiency, thus high figure-of-merit (FoM). Unfortunately, 60 GHz frequency generation in CMOS has typically suffered from poor PN, limited TR, and high power consumption.

Description

Phase noise optimization is the most critical problem for a high-quality oscillator at the mm-wave frequency. The phase noise contribution comes from the active device and the passive device. In the active device, the transistor noise also could be separated into gm transistor introduced noise and current source introduced noise. Considering the limited voltage supply in deep sub-micron CMOS technology, the voltage headroom for transistors and the voltage swing are essential points. However, in an oscillator, the tuning is an important system parameter. The tuning components could be the varactors or capacitor array. The optimization of the quality factor from the tuning component could benefit the oscillator phase noise performance. Besides the active component, the LC tank is the core of an oscillator. However, the inductor quality factor is dropping dramatically in the mm-wave frequency due to the skin effect. The meta slot method is an effective way to improve the tank's Q-factor. By optimizing the active transistors' noise contribution and passive components' quality factor, this oscillator achieves the state-of-art phase noise at 60 GHz with quite wide bandwidth, with better than -98 dBc/Hz phase noise at 1MHz offset.

Results

The chip is measured with the better than -98 dBc/Hz phase noise at 1MHz offset at 60 GHz, and the FoMt is better than -188 at 10MHz offset frequency.

Why EUROPRACTICE?

EUROPRACTICE provides the state-of-art EDA tools. The support during the design team is also great for a state-of-art deep-sub micron technology.

References

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[2] Y. Liu, Z. Li, H. Gao, A 24 GHz PLL with low phase noise for 60 GHz Sliding-IF transceiver in a 65-nm CMOS, VOL 113, Microelectronics Journal, 2021

DVINO: DRAC Vector IN-Order processor

Barcelona Supercomputing Center (BSC), Universitat Politècnica de Catalunya (UPC), Centre Nacional de Microelectrònica (IMB-CNM (CSIC)), Spain
Instituto Politécnico Nacional de México (CIC-IPN), Mexico

E-mails: miquel.moreto@bsc.es, francesc.mollecheto@bsc.es, roger.figueras@bsc.es

Technology: TSMC 65nm
Die size: 2940µm x 2940µm
Design Tools: Cadence: Virtuoso, Genus, Innovus; Siemens: Calibre, Questasim
Application Area: Open-Source Hardware

Introduction

The DRAC project (Designing RISC-V-based Accelerators for next generation Computers) addresses the design, verification, implementation and fabrication of a high performance general purpose processor that incorporates different accelerators based on the RISC-V technology. These accelerators will focus on specific application domains in the field of security, genomics and autonomous navigation.

Description

DVINO is the second generation of the Lagarto processor series [1]. It is a 64-bit RISC-V processor that features one Lagarto Hun core (RV64IMA 5-stage in-order pipeline, 64 BTB, 64 BHT) and one Hydra Vector Processing Unit (VPU). The SoC integrates one Lagarto Hun core, one Hydra VPU, the first Level Instruction and Data caches, the Memory Management Unit (MMU) and a unified L2 cache. Apart from the SoC, several peripherals are integrated to connect the processor with off-chip devices such as SDRAM, HyperRAM, VGA, JTAG, UART and an SD card. Furthermore, the DVINO ASIC includes also a custom developed configurable low-jitter PLL and an ADC.

Lagarto Hun core has support for hardware integer multiply/divide (M extension), atomic memory operations (A extension). As well as the full privileged instruction set extension (version 1.11). It implements a 39 bit, page-based virtual memory scheme (SV39). The design makes use of 5-stage single-issue datapath that executes instructions in program order.

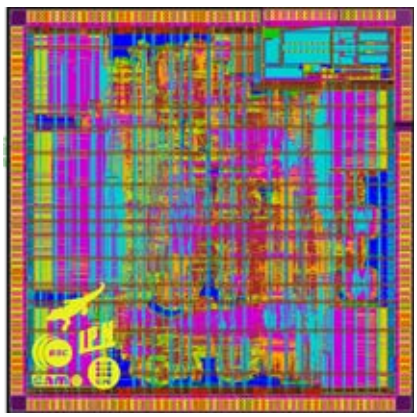

Fig.1: Full layout of the DVINO design.

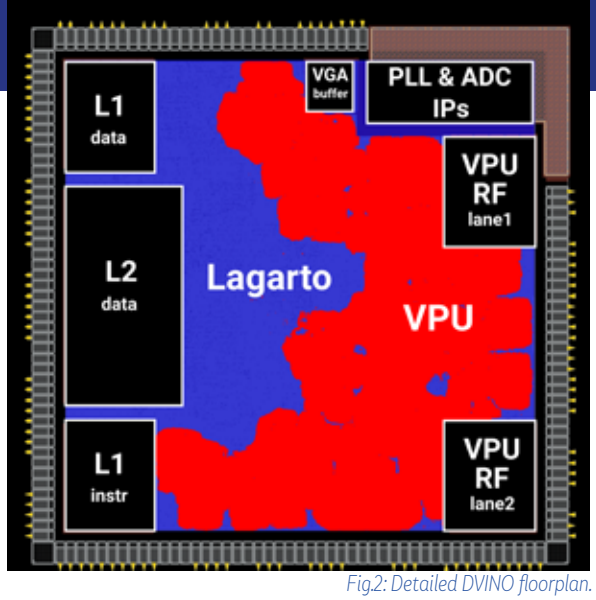

Fig.2: Detailed DVINO floorplan.

Results

DVINO has been fabricated in TSMC 65nm CMOS LP MS/RF (mini@sic). Design size is 2940µm x 2940µm and uses 192 IO pads (including power supply). It is capable (from simulations) to run at a clock frequency up to over 800MHz. Although received samples have been checked to be minimally active, a complete test setup for all the DVINO features is being fabricated including 256MBit Hyperram, 2048MBit SDRAM, and all the peripherals.

Why EUROPRACTICE?

EUROPRACTICE offers affordable services for ASICs prototyping over different advanced technology nodes including constructive and efficient support at both management and technical levels. Moreover, EUROPRACTICE provides access and effective support to EDA tools needed to design such complex chips and SoCs. Finally, its services also include the samples packaging for their further test and characterization at users side. That is why most of the organizations involved in this project have been using EUROPRACTICE services and support for so long and successful time.

Acknowledgements

This work has been funded by the European Union Regional Development Fund within the framework of the ERDF Operational Program of Catalonia 2014-2020, with a grant of 50% of total cost eligible under the DRAC project, with number 001-P-001723.

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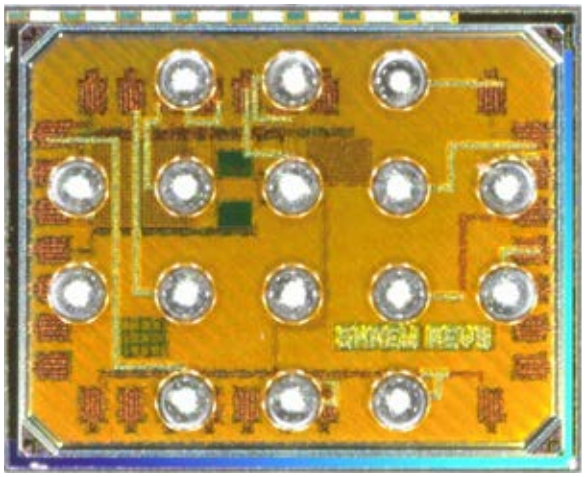

Fig.1: Die micrograph.

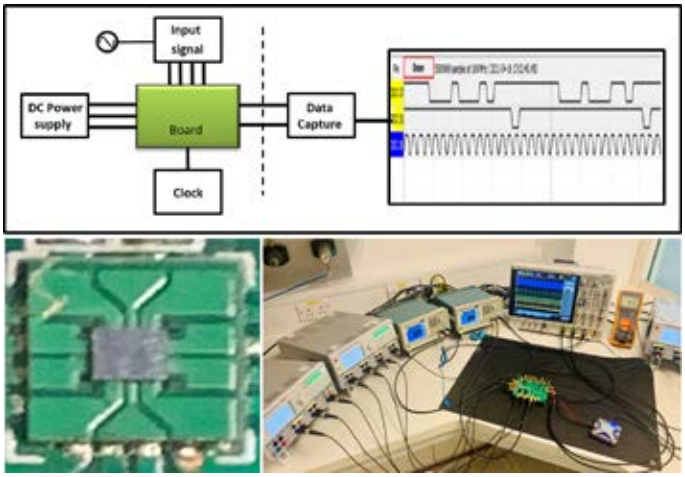

Fig.2: Test measurement setup.

Ultra-low power embedded SAR ADC

Microelectronics Circuit Centre Ireland (MCCI), Tyndall national institute, University College Cork, Ireland

Contacts: Madhan Venkatesh, Gerardo Salgado, Ivan O'connell
E-mail: madhan.venkatesh@mcci.ie
Technology: TSMC 65nm
Die size: 1245µm x 966µm
Application Area: IoT

Description

In energy constrained edge devices, ultra-low power operation is a critical consideration when operating from a lifetime battery or an energy harvesting source. In such applications it is important to ensure that all the sub-blocks are optimally powered, which means that the sub-blocks are provided with just enough energy to complete their task and no more. However, while traditionally this was achieved through the use of multiple power supply rails and a high voltage clock, operating all the circuits from a single supply eliminates the requirement for multiple DC-DC converters or external power supplies enabling a truly low power system approach. The proposed SAR ADC design was fabricated in 65nm CMOS process and packaged using a wafer scale package approach and occupies area less than 0.04 mm^2.

Results

The top part of Figure 2 shows schematic representation of the measurement setup for testing the fabricated SAR ADC.

The bottom left part of Figure 2 shows a close-up picture of the die in the daughter card (chip scale packaging); the bottom right part contains a picture of the Measurement and evaluation setup.

The serial comparator data and EOC signal (which are active low) is taken from the chip and converted in to parallel and processed in Matlab to get the required FFTand has confirmed the expected functionality.

Why EUROPRACTICE?

EUROPRACTICE program offers designers and researchers the opportunity to prototype their designs at an affordable price. EUROPRACTICE staff provide excellent technical support through the different stages of the tape-out.

Acknowledgements

The authors would like to acknowledge the support of ananlog devices. The authors would also like to acknowledge chrisitian Birk, analog devices, cork Ireland and marcel Pelgrom, Eindhoven, Netherlands for their valuable input and technical discussions.

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Wireless Power Transfer System with Light-Load Efficiency Enhancement and Instant Dynamic Response for Bioimplants

Iowa State University, USA

Contacts: Junyao Tang, Lei Zhao and Cheng Huang
E-mail: chengh@iastate.edu

Technology: TSMC 0.18µm CMOS Mixed-Signal/RF
Die size: Two chips: 1625µm x 600µm (TX) and 1625µm x 800µm (RX)
Application Area: Medical / Health

Introduction

Wireless power transfer (WPT) systems are becoming increasingly popular for sub-100mW biomedical applications, such as cochlear implants, retinal prostheses, or brain machine interfaces. Because the received power is sensitive to coupling and loading conditions, power/voltage regulations are essential to achieve stable and accurate power delivery, fast transient response, and high end-to-end (E2E) efficiency, which includes all the power losses in the transmitter (TX), wireless power link, and the receiver (RX). However, many existing WPT designs operated in open-loop; or achieved voltage regulation but only in the RX, with the TX remained unregulated and designed to operate at fully capacity, thus degraded E2E efficiency at light-load conditions. Because lower-power or standby mode typically contributes to the majority of the operation time, light-load efficiency is always an important specification of power management circuits, especially to extend the run time for battery-powered devices, e.g., a wearable/portable WPT transmitter supporting bioimplants. There are previous designs in the literature reported different approaches to achieve TX regulation; however, they all required extra discrete components, which increased the form-factor and cost, with some even required a wire to close the loop. The reported dynamice performance (e.g., load transient reponse) was also relatively slow.

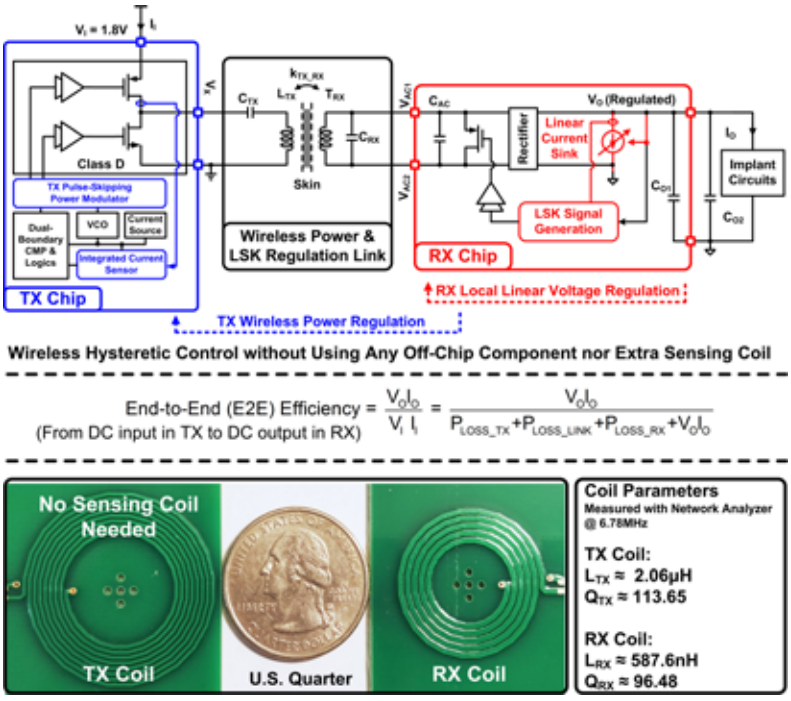

Fig.1: System block diagram of this wireless hysteretic controlled WPT system.

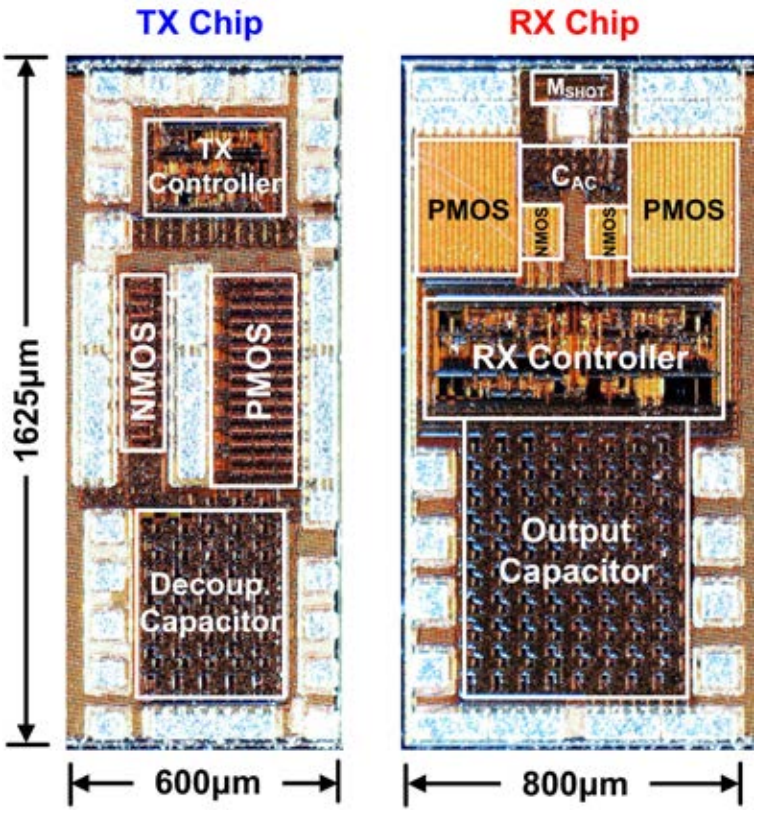

Fig.2: Chip photos of both the TXand RX chips.

Description

In ISSCC 2021, we presented a complete WPT system [1] with fully-integrated wireless hysteretic control to achieve both RX local voltage regulation and TX wireless power regulation with instant load-transient response and enhanced E2E light-load efficiency. The wireless power regulation is achieved without using any off-chip components, wires nor coils, and the straightforward hysteretic operation is intrinsically stable and insensitive to parasitics and variations.

The proposed WPT system includes: two chips, the RX and TX chips; and two power coils on PCBs, with a smaller RX coil and a larger TX coil for better alignment tolerance. Two levels of regulations: voltage regulation locally in RX and power regulation wirelessly thorough TX, are achieved. Details can be found in [1].

Results

According to the measurement results, our system achieved: 1) stable TX and RX voltage/power regulation with instant dynamic response, without using any off-chip components nor wires; 2) up to 20% light-load efficiency enhancement compared to state-of-the-art with the new wireless hysteretic control; 3) eliminates the need for a current sensing coil for LSK signal generation, which reduces the PCB area by 86%.

Why EUROPRACTICE?

EUROPRACTICE provides stable and affordable MPW runs for universities. The supervisor of this project is a long-term user of EUROPRACTICE Services, back in the time when he was a student. The technical staffs are also very responsive and helpful.

References

[1] J. Tang, L. Zhao, and C. Huang, "33.6 A Wireless Power Transfer System with Up-to-20% Light- Load Efficiency Enhancement and Instant Dynamic Response by Fully Integrated Wireless Hysteretic Control for Bioimplants," in 2021 IEEE International Solid- State Circuits Conference (ISSCC), Feb. 2021, vol. 64, pp. 470–472. doi: 10.1109/ISSCC42613.2021.9365859.

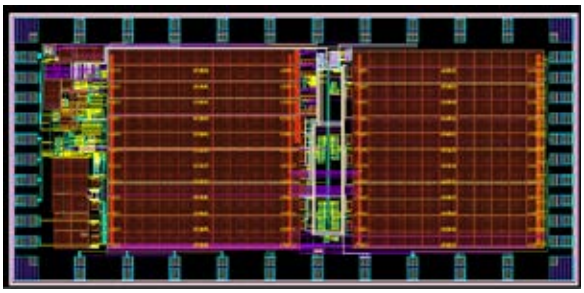

Fig 1: Chip Layout

Power management system for microscale energy harvesting

Cairo University, Egypt

Contacts: Dr. Ahmed Nader Mohieldin, Eng. Basem A. Abdelamgid, Eng. Mahmoud H. Kamel
E-mail: anader@eng1.cu.edu.eg

Technology: UMC L180 MM/RF
Die size: 3240µm x 1525µm
Application Area: Energy

Introduction

Energy harvesting sources have been recently emerging as a promising power source that can be used in low-power portable systems such as Internet of Things (IoT) and biomedical implanted devices. In such systems, these sources after proper signal conditioning can be either used to directly power the circuits of the application or to recharge small batteries that can be later used for the same purpose.

Description

In this work, a power management system for microscale energy harvesting was implemented with the aim of maximizing efficiency and minimizing redundancy. Two architectures have been proposed. The first architecture is an adaptive dual output system with maximum power point tracking (MPPT) and storage capability. The first output delivers the load power and is regulated at 1.6 V. This output is provided by the primary path of the system that is implemented using a 5-stage reconfigurable Dickson charge pump. In case of the presence of more available power than the load demand, a secondary path is enabled to store the excess amount of energy on a supercapacitor. This provides the second output of the system that is capable of charging up to about twice the voltage of the first output. Besides storing the excess energy, the secondary path also helps in regulating the first output and achieving the MPPT of the input source.

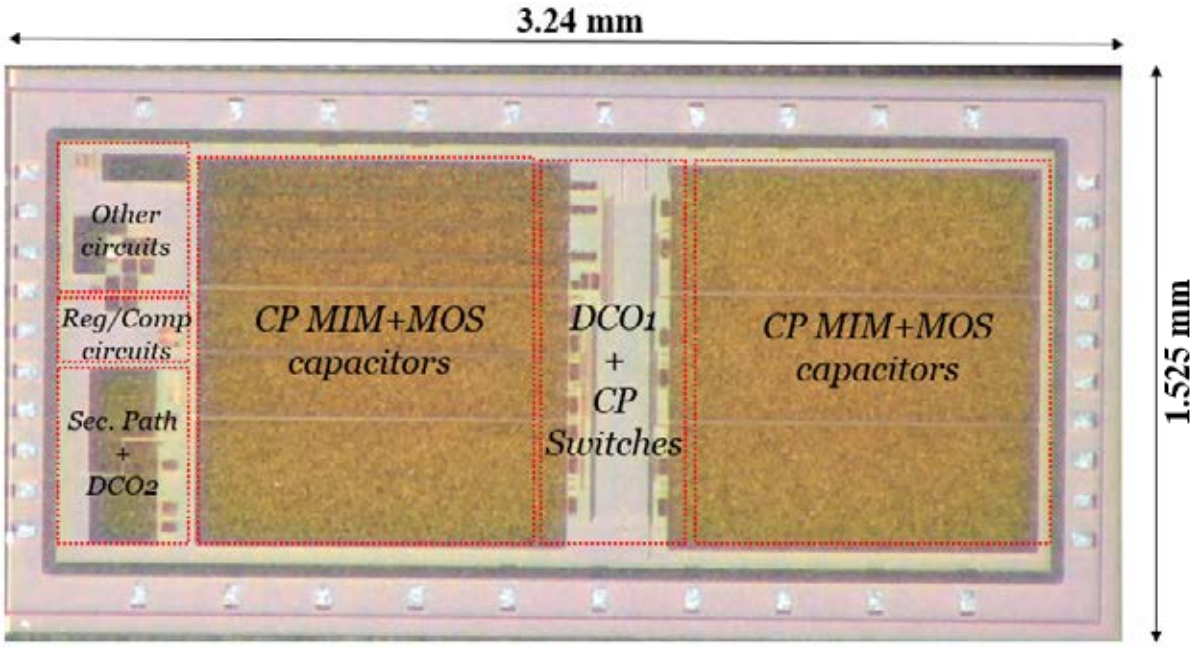

Fig 2: Chip Micrograph

The second architecture provides a regulated output voltage of 1.5 V using a DC-DC charge pump (CP). The proposed CP can provide fractional voltage conversion ratio (VCR) in a step of 0.25 to support wide input range from 0.4-1.2 V. The system efficiency is optimized using a real-time monitoring for the input current supplied to the CP. The proposed system is reconfigured, with the aid of a finite state machine, to maximize the end-to-end efficiency. This is achieved by adaptively optimizing the number of stages and switching frequency that provides the required constant output voltage.

Results

The proposed system utilizes a total on-chip flying capacitance of 2.4 nF. Measurement results show that the system achieves an end-to-end efficiency of more than 70% at a total output power around 1 mW, while supporting self-start-up.

Why EUROPRACTICE?

The EUROPRACTICE ASIC team has helped to revise the GDS to make sure that all foundry checks are met. EUROPRACTICE has also handled the packaging of the fabricated dies for final delivery to us.

Acknowledgements

This work was supported by the Information Technology Industry Development Agency (ITIDA) under Grant PRP2018. R25 (CFP 150).

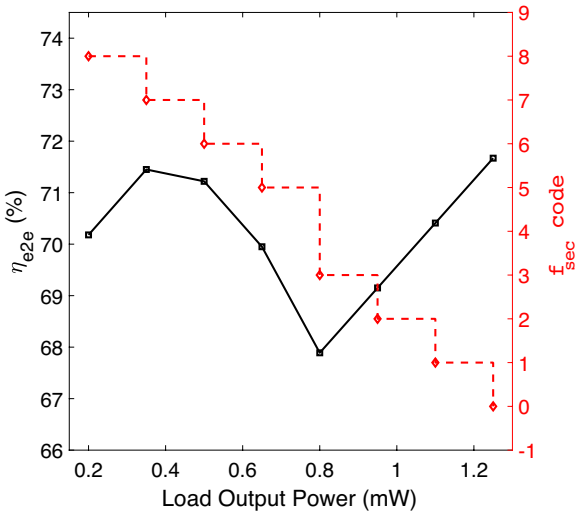

Fig 3: Efficiency of first architecture

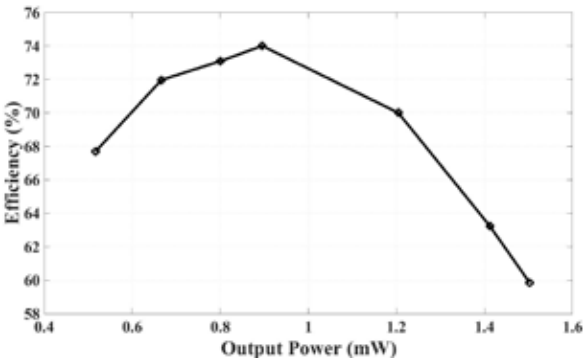

Fig 4: Efficiency of second architecture

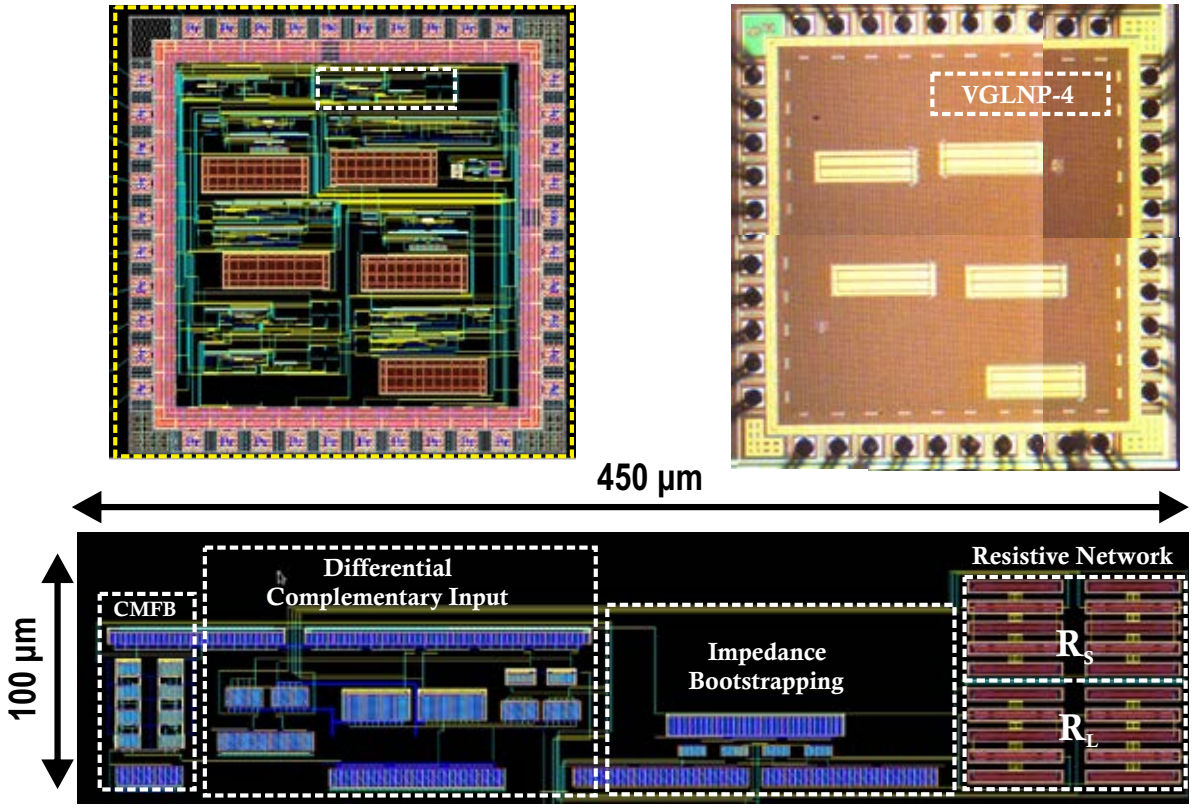

Fig.1: Microphotograph of the chip including the layout of the proposed circuits.

Low-Noise Chopper Amplifiers for Signal Conditionings Sensors

National Institute for Astrophysics, Optics and Electronics (INAOE), Mexico
Public University of Navarra (UPNA), Spain

Contacts: Oscar-Cinco, María-Sanz, Carlos-De la Cruz
E-mail: oscar.cinco@inaoep.mx
Technology: UMC L180 MM/RF
Die size: 1500µm x 1500µm
Application Area: Sensors / Transducers

Introduction

The use of wireless sensors has opened countless applications in almost all fields, from industry and science to entertainment, household and security. The realization of signal preprocessing systems has become a major challenge, as they must comply with strict requirements not to degrade the performance of the whole portable system. The analog front-end of an interface circuit connected directly to the sensing element has to transform the raw sensor signal into a signal suitable to be processed by the subsequent A/D converter. The preamplifier functions are normally limited to amplification and filtering, leaving more complex signal processing tasks to the digital section. The device has been created to implement signal conditioning systems of sensors to handle signals in order of microvolts.

Description

There are two different approaches to reduce flicker noise. The first approach is through circuit topology and transistor sizing. It can be used to amplify signals of at least tens of microvolts. The second method is the use of dynamic offset cancellation techniques, which can be classified into two groups: auto-zero and chopping.

In this chip, several low-noise circuits have been designed using the chopping technique. These designs include different kind of circuits. First, the design of voltage preamplifiers by analysing and reducing the noise contribution of the devices through both large sizing and topology modifications. Second, implementation of fully integrated Gm-C low-pass filters with low cut-off frequency, in particular taking advantage of the bootstrapping technique to reduce the cut-off frequency in a range from hundreds of Hz to tens of kHz. Combination of the above presented blocks to design low-noise chopping amplifiers. They are accessible individually for their characterization.

Results

Several low noise chopping preamplifiers were implemented in this device. All of them are designed to reduce noise contributions at a topological level, and are based on a voltage-current conversion input stage and a current-voltage output conversion stage, to obtain a well-defined gain.

The preamplifier was fabricated in 0.18µm CMOS technology. The chip microphotograph and layout are shown in Figure 1. The area of the circuit is 450µmx100µm, which includes the preamplifier as well as the CMFB circuit. Figure 2 shows the test bench for the experimental characterization. Figure 3 shows the frequency response for different gains.

Furthermore, the input-referred noise and the THD were characterized. In this way, it was possible to determine Figures of Merit (FoMs) to compare the performance with another approaches. The proposed circuits achieve FoMs that are competitive with those presented in the state of the art.

Why EUROPRACTICE?

The National Institute for Astrophysics, Optics and Electronics (INAOE) has worked with EUROPRACTICE for several years. EUROPRACTICE Services provide access to design support and process design kits. Besides, EUROPRCATICE offers excellent technical support for DRC verification and GDS submission. Finally, EUROPRACTICE provide access to different technologies at affordable price.

Acknowledgements

This work was supported by CONACYT through the Doctoral Grant 467255 and the Research Project CONACYT CB-2015-257985.

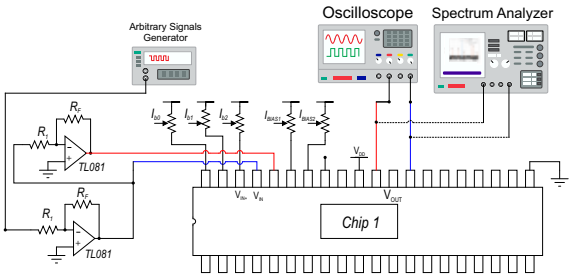

Fig.2: Test bench for experimental characterization.

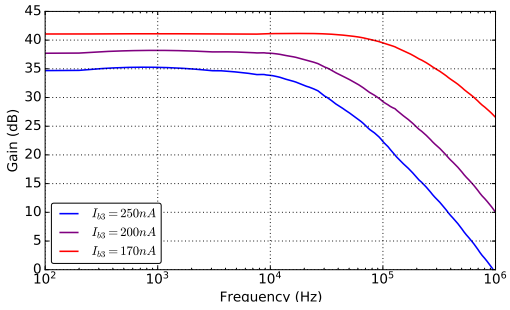

Fig.3: Frequency response of the Variable Gain Low-Noise Preamplifier.

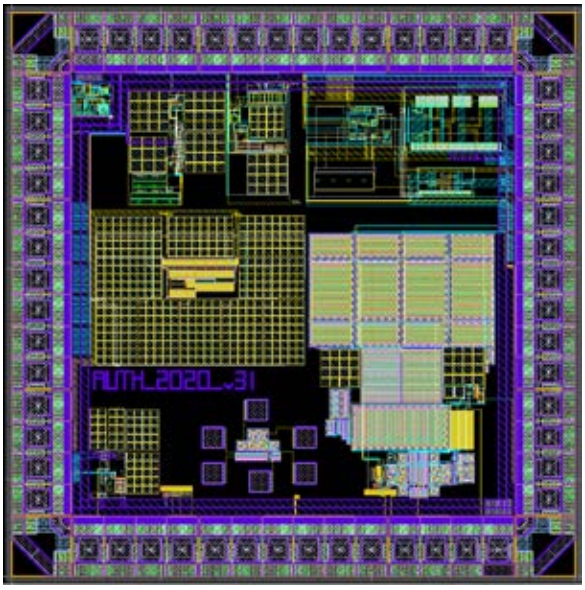

Fig.1: Layout view of SmartPV.

Cell-level Energy Management IC for Smart Photovoltaic plants

Electronics Lab., Physics Department, Aristotle University of Thessaloniki, Greece

Contacts: Vasiliki Gogolou, Zoi Agorastou
E-mails: vgogolou@physics.auth.gr, zagorast@physics.auth.gr

Technology: X-FAB XH018
Die size: 1520µm x 1520µm
Design Tools: Cadence: Spectre, Virtuoso, Assura, PVS
Application Area: Energy

Introduction

During the last years there is an increasing demand for the utilization of solar energy for electric-energy generation purposes. A rapid increase of the installed Photovoltaic (PV) capacity has been performed both in the European Union and outside Europe over the last 10 years and it is expected to continuously expand.

In the framework of the project SmartPV - "Development of a Smart Photovoltaic Cells system" (https://smartpv.gr) an innovative system that is responsible for the management of the energy produced from photovoltaic cells is implemented. The breakthrough of the Smart Photovoltaic Cells is that they comprise an integrated circuit (IC) that manages and processes the available power at the PV cell level in contrast to conventional PV systems that perform the energy management process in arrays of PV cells/panels.

The final IC will be responsible for the maximization and management of the energy produced by each solar cell, the detection of malfunctions as well as the remote (through the power lines) control and monitoring of each Smart Solar Cell.

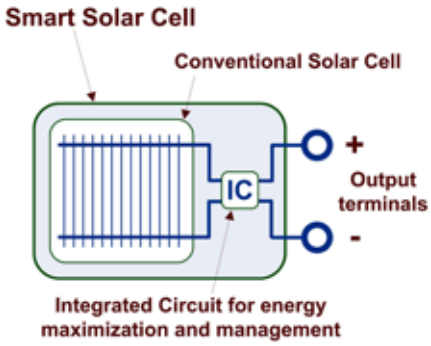

Fig.2: Smart Solar Cell.

Description

The proposed system consists of a DC-DC converter responsible for the efficient conversion of the PV cell power and the production of a regulated DC output voltage. Next, a DC-AC converter fed by this DC output voltage provides an AC output. A number of Smart Solar Cells can be connected in series in order to provide a sinusoidal output at the appropriate voltage level. In addition, several supplementary low-power analog circuits were designed, both for the control of the DC-DC and the DC-AC converters and to provide information to the digital part of the system which is in charge of the Maximum Power Point Tracking (MPPT) process.

This particular mini@sic tapeout process was conducted in order to test the analog control circuits for the energy management of the PV cells, such as the PV voltage and current sensors providing digital output for the digital MPPT unit, a ring oscillator generating the clock for the digital part of the system, the drivers for the DC-DC and DC-AC converters, an LDO and finally a cold-start circuit that is based on a charge-pump for the start-up of the system.

Results

The circuits were tested with successful results since the voltage and current sensors produce a digital output proportional to their input in a large range. Also, the ring oscillator in conjunction with the drivers, as well as the cold start units, are operating properly.

Why EUROPRACTICE?

Aristotle University of Thessaloniki has an ongoing partnership with EUROPRACTICE since 1996. Through EUROPRACTICE we obtain access to multiple state-of-the-art IC technologies - such as XH018 which is used in this case - design tools and low-cost prototyping, key features for the progress of our research and educational tools for our students. Furthermore, imec's technical support has been proven crucial for the successful GDS submissions of our designs through the years.

Acknowledgements

This research has been co-financed by the European Regional Development Fund of the European Union and Greek national funds through the Operational Program Competitiveness, Enterpreneurship and Innovation, under the call RESEARCH-CREATE-INNOVATE (project code: T1EDK -01485).

On-chip digital MPPT control for energy harvesting applications

Electronics Lab., Physics Department, Aristotle University of Thessaloniki, Greece

Contacts: Vasiliki Gogolou, Ioannis Mandourarakis, Emmanouil Kavvousanos
E-mail: vgogolou@physics.auth.gr

Technology: X-FAB XH018
Die size: 1520μm x 1520μm
Design Tools: Cadence Virtuoso, Genus, Innovus and PVS
Application Area: IoT

Introduction

Nowadays, the energy harvesting concept is widely adopted in order to fulfil the energy demands of millions IoT devices. The main concern is the constant and reliable power supply of the system. However, the energy extracted from harvesters such as photovoltaic (PV) cells, thermoelectric generators (TEGs) etc. varies with both the ambient operating conditions (e.g. ambient temperature, solar irradiation etc.) as well as the output load, leading to poor overall power conversion efficiency. To this end, Maximum Power Point Tracking (MPPT) systems are used in order to extract the maximum possible energy from the power source during the continuously changing ambient and load operating conditions.

Traditionally, MPPT techniques are implemented in energy harvesting systems using microcontrollers or FPGA devices. However, with the advancement of the IoT field and the minaturization of the devices, the on-chip integration of MPPT techniques is crucial.

Description

To this end, an integrated MPPT control system is implemented (Fig 1). The Perturbation and Observation (P&O) technique has been selected since it combines the advantages of operational

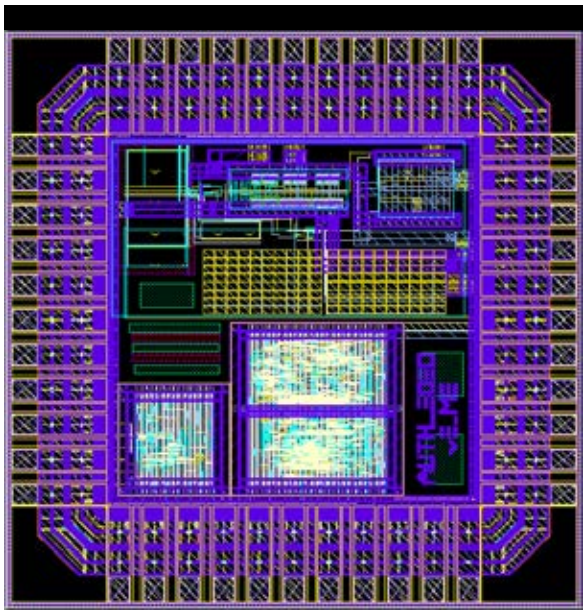

Fig.1: Physical design of the chip.

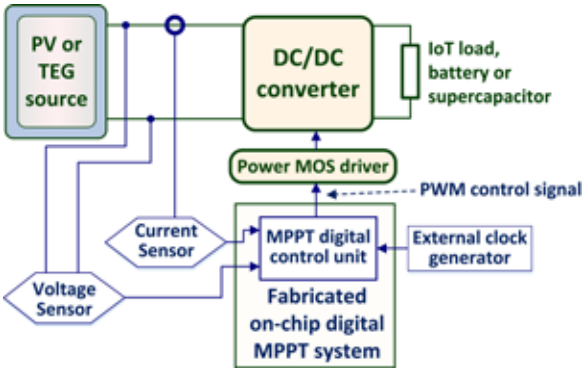

Fig.2: A block diagram of an IoT energy harvesting system employing the fabricated on-chip MPPT control system.

simplicity and efficient operation. The proposed MPPT control system is utilizing only digital circuits, thus avoiding the need of high-complexity and/or analog circuits such as multipliers, A/D converters etc. which exhibit a relatively high power consumption. Thus, the on-chip integration is easily achieved and a simple and elegant solution is implemented.

Results

In order to evaluate the performance of the fabricated on-chip MPPT controller, an experimental PV energy harvesting system was constructed according to Figure 2. Two voltage and current sensors, providing digital output, were connected to the inputs of the MPPT block. Its PWM output is connected to the drivers of a Boost DC/DC converter. The input PV source was installed outdoors and its power-voltage curve was measured experimentally as shown in Figure 3. Then, the fabricated MPPT system was set to operate, resulting in convergence to the operating point (Figure 3), where the power produced by the PV source is maximized.

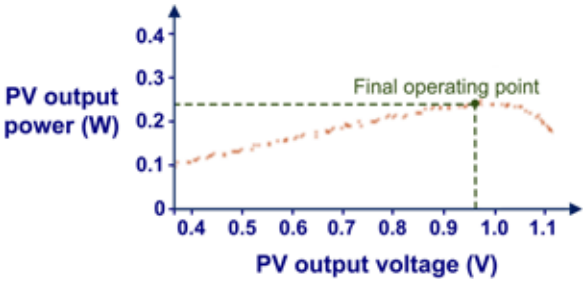

Fig.3: The experimentally measured power-voltage curve of the PV source during testing the fabricated on-chip MPPT system and the final operating point.

Why EUROPRACTICE?

Aristotle University of Thessaloniki has an ongoing partnership with EUROPRACTICE since 1996. Through EUROPRACTICE we obtain access to multiple state-of-the-art IC technologies - such as XH018 which is used in this case - design tools and low-cost prototyping, key features for the progress of our research. Furthermore, imec's technical support has been proven crucial for the successful GDS submissions of our designs through the years.

Acknowledgements

This research has been co-financed by the European Regional Development Fund of the European Union and Greek national funds through the Operational Program Competitiveness, Entrepreneurship and Innovation, under the call RESEARCH – CREATE – INNOVATE (project code:T1EDK-00360)

The contribution of Mr. Kleanthis Papachatzopoulos in the synthesis of the physical design is acknowledged.

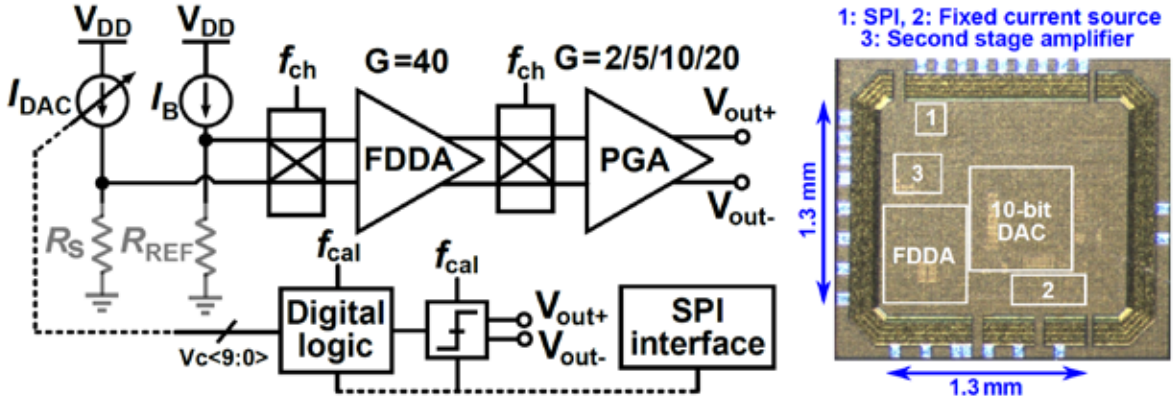

Fig.1: System level block diagram of the readout chip and its micrograph (adapted from [1]).

An ultra-low-noise frontend for magnetoresistive sensors

Institute of Smart Sensors,
University of Stuttgart, Germany

Contacts:	Ayman Mohamed, Jens Anders
E-mail:	ayman.mohamed@iis.uni-stuttgart.de
Technology:	X-FAB XT018
Die size:	1.7 mm²
Design Tools:	Cadence: Spectre, Innovus, Genus, Assura and PVS
Application Area:	Medical / Health

Introduction

Point of care (PoC) bisosensing systems are a very active field of research that gained tremendous momentum in the last two years due to the Covid pandemic. Magnetoresistive (MR) sensing systems present a very promising route towards cos-effective, yet very affordable biosensing platforms. Apart from limitations in the sensor itself, the performance of existing MR sensing systems is mostly limited by the sensor interface electronics. Therefore, our work focuses on the design of an ultra-low-noise MR frontend that can bias the MR sensor, compensate for its offset, and amplify the minute voltage signals representing the biosensing signals with minimum degradation of the intrinsic sensor SNR.

The presented chip can be incorporated into low-cost PoC MR systems that can be used to diagnose different diseases with high specificity and sensitivity while keeping the testing costs affordable. With their low cost and ease of operation, such MR sensor systems can target both markets in developed and developing countries.

Description

This chip architecture as well as its micrograph are shown in Figure 1 [1]. It features an ultra-low-noise 10-bit current-mode digital-to-analog converter (DAC) to bias the MR sensor(s). The DAC provides currents up to 1 mA to compensate offsets originating from background magnetic fields or due to the spread in the MR base resistance. This is achieved by continuously monitoring the voltage difference between the MR sensor and the reference resistor. The automatic

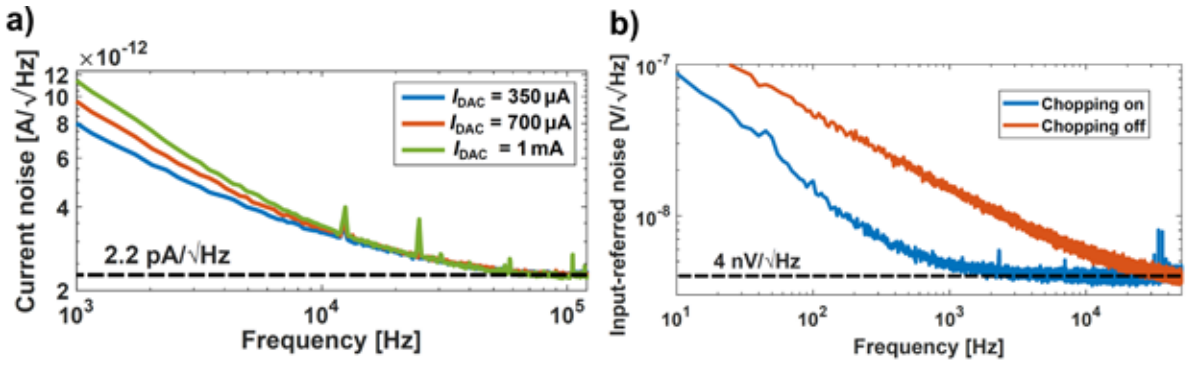

Fig.2: a) Measured current noise PSD of the current bias for different current settings;
b) Measured input-referred voltage noise PSD of the amplifier chain with and without chopping (adapted from [1]).

calibration routine is triggered via an on-chip SPI interface. Afterwards, the voltage signal of the MR sensor is amplified by a fully differential difference amplifier (FDDA) followed by a programmable gain amplifier. The FDDA incorporates chopping switches to mitigate its offset and 1/f-noise.

Results

The current noise power spectral density (PSD) of the current DAC bias as well as the input-referred voltage noise PSD of the amplifier chain are shown in Figure 2. The current bias achieves a state-of-the-art noise floor of 2.2 pA/√Hz for different current settings, cf. Figure 2a. Moreover, the measured noise floor of the amplifier chain is 4nV/√Hz with a chopping-enabled low 1/f-corner frequency of 400 Hz, cf. Fig. 2b. The measured performance of the chip including its input noise is in very good agreement with the post-layout simulations. This verifies the high accuracy of the XT018 models provided by X-FAB via EUROPRACTICE.

Why EUROPRACTICE?

The University of Stuttgart has been working closely with EUROPRACTICE over the last years on fabricating state-of-the-art IC designs requiring many different types of technology nodes with reliable technology models. EUROPRACTICE has been providing us with a very diverse PDK portfolio covering all design aspects, while constantly updating their portfolio with the latest technology nodes. Moreover, the EUROPRACTICE technical support team is constantly exceeding our expectations with very fast response time to solve any technical problem even shortly before tapeout dates. Finally, the prices offered by EUROPRACTICE, for design tools and manufacturing are very attractive and represent a key enabler for research institutes to be able to stay in the IC design business.

Acknowledgements

This work is supported by the Carl Zeiss Foundation and the German Research Foundation (DFG) under contract no. AN 984/12-1.

References

[1] A. Mohamed, H. Heidari, and J. Anders, "A readout circuit for tunnel magnetoresistive sensors employing an ultra-low-noise current source," in ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), 2021, pp. 331–334.

CLAROC : A chip to provide precise calibration pulses for ATLAS calorimeter detector at CERN

Centre de micro-electronique OMEGA – CNRS/ IN2P3-Ecole Polytechnique, Palaiseau, France

Contact: Gisele Martin-Chassard
E-mail: gisele.martin-chassard@in2p3.fr
Technology: XFAB XT018
Die size (nm): 2 times 2mm x 2.8mm
Application Area: High Energy Physics (HEP)

Introduction

The CLAROC ASIC will provide the calibration of the electromagnetic calorimeter for ATLAS experiment at CERN. The goal of the circuit is to generate variable high precision (0.1%) test pulses in each measurement channel of the detector over the whole energy range (from 5µA to 320mA).

Description

The chip shows two dies. Each one embeds four high-frequency switches to provide four calibration channels as shown in Figure 1. One die has 4 identical channels and the other one has 4 different channels in order to test different transistor types and different ground paths.

The high-frequency switch receives a very precise current from 5µA to 40µA. By a variable gain from 1 to 8, it provides a precise current from 5µA to 320mA on an external self and resistor to obtain a variable pulse.

Thanks to X-FAB 10V transistors, we could make the high frequency switches for which the output pulse could reach 8V on 25 Ohms load. The 6 metal levels are very efficient to drive properly a relative high current and to obtain good uniformity between the four channels.

Results

The two dies are packaged in QFN100 case. The tests show good results in terms of dynamic range and linearity for the switch part, but more mitigated results for the variable gain. The chip, which will be used in high energy physics experiment, has been characterized in irradiation environment. Irradiation tests were performed in X-ray beam up to 3Mrad at CERN and in proton beam until 4 Mrad using Proton Irradiation Facility (PIF) of Paul Scherrer Institute (PSI).

These tests show an important Vt shift for standard 5V

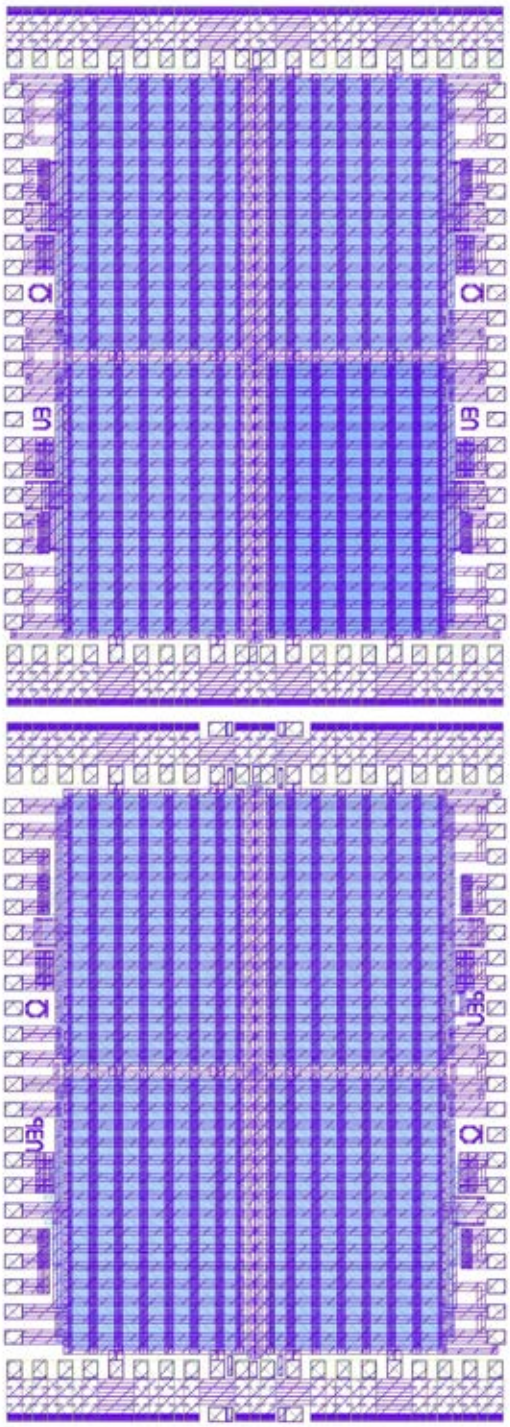

Fig.1: CLAROC layout.

MOS. This leads to unacceptable non-uniformity on the variable gain to maintain the precision imposed in CERN experiments. However, the results are acceptable for 10V MOS transistors. Seeing these results, we are redesigning the switch so that the shift of the Vt doesn't affect the precision of the output current. The new chip will be submitted in a next run.

Why EUROPRACTICE?

EUROPRACTICE MPW program offers designers and researchers the opportunity to prototype their designs at an affordable price. EUROPRACTICE staff provide excellent technical support through the different stages of the tape-out.

Optical Phased Array for optical wireless communication and 3D sensing

Integrated Photonic Devices Group, Faculty of Electrical and Computer Engineering Technical University Dresden, Germany

Contact:	Shahryar Sabouri
E-mail:	shahryar.sabouri@tu-dresden.de
Technology:	AMF Si-Photonics (AMF-QP-RND-002)
Die size:	16mm x 3.2mm
Design Tools:	Synopsys OptoDesigner
Application Area:	Datacom / Telecom

Introduction

This device enables optical wireless communication and 3D sensing at the same platform which can be used for telecom data link applications and LiDAR systems.

Description

This device is an optical phased array including 64 waveguide gratings optimized for a large emission length in C-Band. Two steps of phase controlling are considered for a wide beam steering and splitting in a high spatial resolution.

Why EUROPRACTICE?

The technology offers a high resolution of passive and active devices on the same Silicon Photonic Chip including Edge couplers, local trench, PDs, and very energy-efficient thermo-optical phase shifters.

Acknowledgements

This work is supported in part by the Federal Ministry of Education and Research (BMBF) in the context of Fastoptics project.

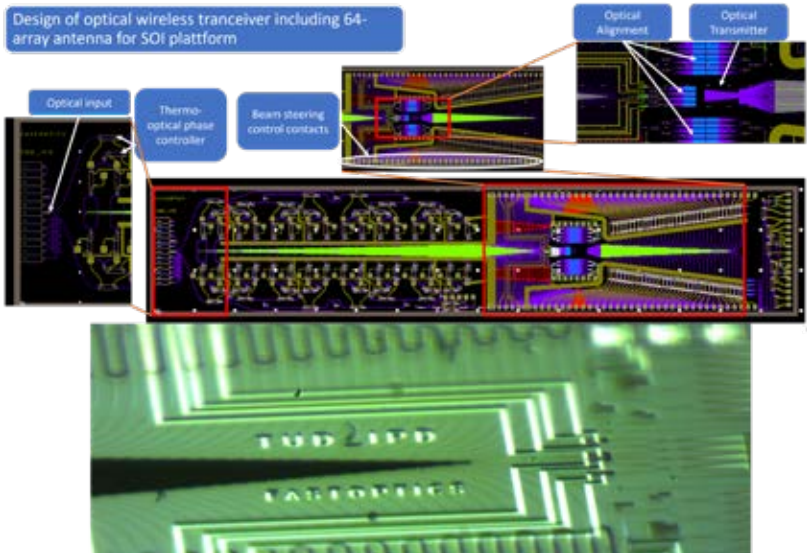

Fig.1: Structure of the fabricated optical phased array.

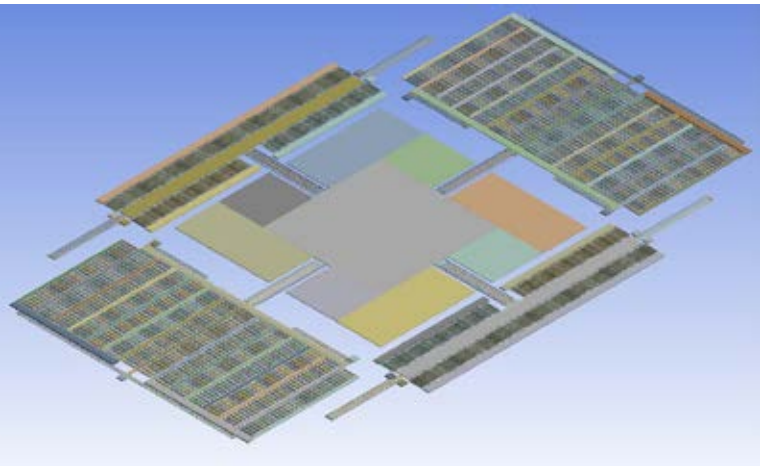

Fig.1: 3d-model of integrated two-axis MEMS gyroscope-accelerometer.

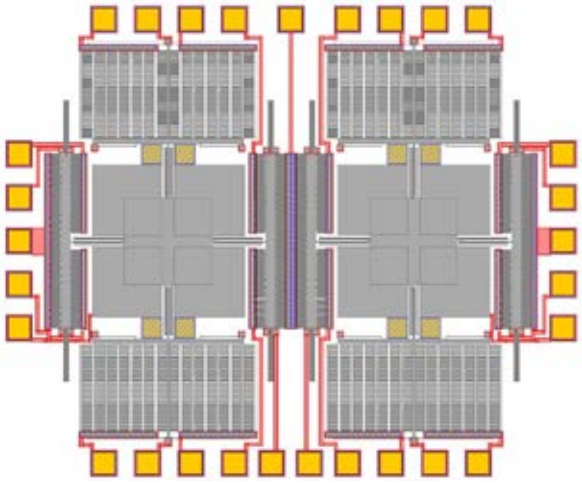

Fig.2: Layout of integrated two-axis MEMS gyroscope-accelerometer

A Two-Axis MEMS Gyroscope-Accelerometer manufactured by Technology of PolyMUMPs

Design center for microelectronic component base for artificial intelligence systems, Southern Federal University, Taganrog, Russia

Contact: Igor E. Lysenko
E-mail: ielysenko@sfedu.ru

Technology: PolyMUMPs
Die size: 4.8mm × 4.8mm
Design tools: Siemens L-Edit
Application Area: Smart Mobility

Introduction

Design center for microelectronic component base for artificial intelligence systems of the Southern Federal University is developing a system for monitoring, diagnostics and predicting of rail track defects. This system is a stand-alone device and is mounted on a wagon bogie. It includes various sensors, as well as a two-axis MEMS gyroscope-accelerometer. The signals of the MEMS gyroscope-accelerometer are processed using artificial neural networks.

Description

The MEMS gyroscope-accelerometer was fabricated using MEMSCAP's PolyMUMPs Process. This work is part of a Ph.D+ research study by Mark Denisenko on the design of two-axis MEMS gyroscope-accelerometer to explore the feasibility of his theoretical concept. These MEMS gyroscope-accelerometer were analytically studied and simulated using ANSYS. The topology of the device is designed in the editor L-Edit, Tanner. The main feature of the developed MEMS sensor is that elastic suspensions, proof mass, electrostatic movable and fixed combs drivers, fixed electrodes of transducers are all made in a single structural layer. Using two suspensions allows to exclude mutual influence of primary and secondary oscillations of MEMS gyroscope-accelerometer. The original solutions incorporated in the design of our MEMS gyroscope-accelerometer allow you to simultaneously register rotation and acceleration along two-axis.

Why EUROPRACTICE?

EUROPRACTICE provides excellent prototyping capabilities for integrated circuits and MEMS. It gives access to modern semiconductor processes of the world's largest foundries. The service works quickly and at affordable prices. Excellent technical support from EUROPRACTICE engineers accompanies your project at all stages of design and fabrication.

Acknowledgment

The work was carried out at the expense of funds, task No. FENW-2020-0022 for the implementation of scientific research carrying out scientific research at the expense of the Federal budget, in terms of scientific activities on the topic "Development and research of methods and means of monitoring, diagnostics and forecasting state of engineering objects based on artificial intelligence"..

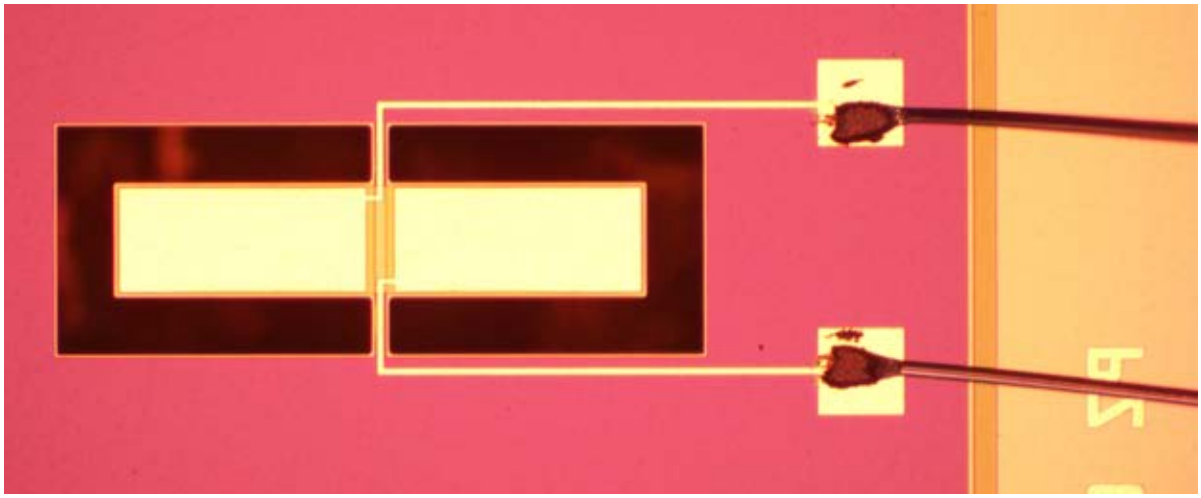

Fig.1: Close up photo of double free cantilever.

Integrated oscillator and amplifier for biomedical devices

Christian-Albrechts-Universität zu Kiel, Networked Electronic Systems, Kiel, Germany

Contacts:	Robert Rieger, Benjamin Spetzler, Patrick Wiegand
E-mails:	rri@tf.uni-kiel.de, benjamin.spetzler@tu-ilmenau.de, pw@tf.uni-kiel.de
Technology:	PiezoMUMPs
Die size:	11mm x 11mm
Design Tools:	Cadence Virtuoso
Application Area:	Medical / Health

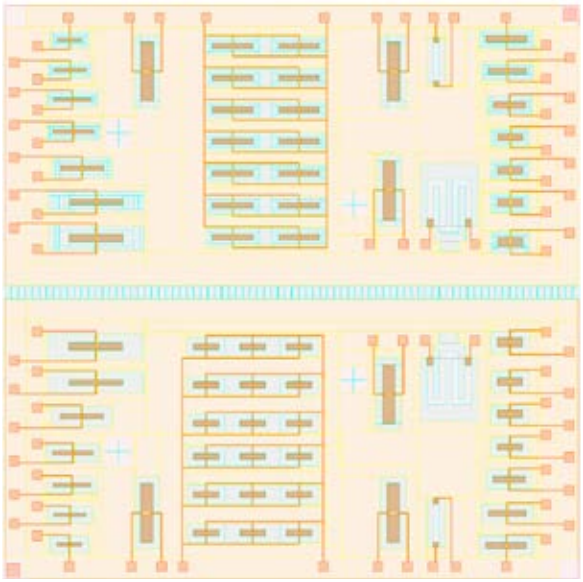

Fig.2: Layout of the MEMS design.

Introduction

With more sophisticated means of measuring heart and brain activity by magnetic fields, magnetic sensors need to get small and sensitive enough for biomedical signals. DeltaE effect cantilever sensors show the potential to match these criteria. The piezoelectric cantilevers get excited in resonance while the surrounding magnetic field modulates the carrier.

Description

The double free cantilevers are designed such, that an additional magnetostrictive layer can easily be applied. This magnetic layer changes its stiffens according to the surrounding magnetic field. Thus, the resonance frequency is changed and the excitation signal is modulated. This effect can be exploited to measure a magnetic field.

Results

Different cantilever sizes were designed to get a measure for the process accuracy, showing deviations of less than 1% in resonance frequency between cantilevers of the same size. The magnetic material is also applicable and showed a reaction to surrounding magnetic fields.

Why EUROPRACTICE?

CMP / EUROPRACTICE provide a clear and easy-to-use web interface for design registration, submission, and queries. The staff is supportive, knowledgeable and easy to contact. The research group has been satisfied with CMP / EUROPRACTICE's services for many years.

Acknowledgements

This research was funded by the German Research Foundation (DFG) via the collaborative research center CRC 1261.

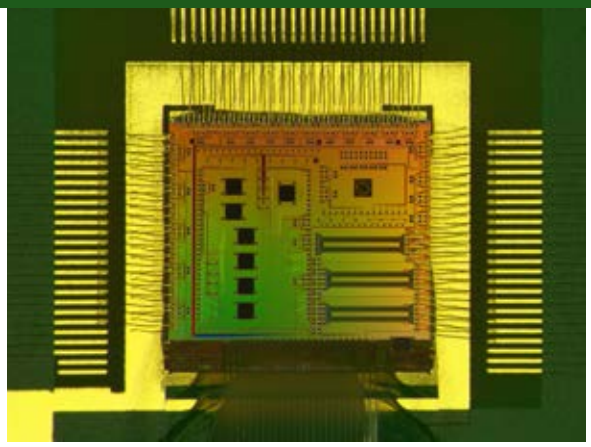

Fig.1: Micrograph of the fabricated PIC wire bonded onto a test board and pigtailed with a 24-channel single-mode fiber array.

Silicon Photonics for High-Energy Physics

Experimental Physics Department, CERN, Geneva, Switzerland

Contacts:	Carmelo Scarcella, Jan Troska
E-mail:	jan.troska@cern.ch
Technology:	imec Si-Photonics iSiPP50G
Die size:	5.1mm x 5.1mm
Design Tools:	Synopsys OptoDesigner
Application Area:	High Energy Physics (HEP)

Introduction

Optical data links are fundamental for High-Energy Physics Experiments. They are used to transfer the data generated by the particle detectors to the off-detector processing electronics. Nowadays, tens of thousands of optical links based on discrete optoelectronics are deployed in the CERN Experiments. Future particle detector upgrades involve a larger data volume produced by the particle collisions and higher levels of radiation resistance will be required for the front-end optoelectronics.

Optical links based on Silicon Photonics (SiPh) offer several advantages. For example, it would be possible to co-integrate the optical transceivers with the Silicon particle sensors.

CERN detectors operate in a radiation environment, and the radiation tolerance of SiPh transceivers can potentially be as good as the sensor and the front-end CMOS electronics. Moreover, the wide bandwidth of Si modulators and Ge photodiodes supports the high data rate that is foreseen in the next generation of particle detectors.

Description

A Photonic Integrated Circuit (PIC) has been designed at CERN and fabricated using the imec iSiPP50G technology through an EUROPRACTICE multi-project wafer (MPW) run. The PIC includes: imec building blocks, CERN custom designed test structures with enhanced radiation resistance, and optical circuits enabling in-lab data transmission experiments. Our development targets a 4-channel Wavelength Division Multiplexing (WDM) link based on µ-ring modulators each one operating at 28 Gb/s.

Results

The PIC prototypes were delivered to CERN in June 2020 and the experimental results are very promising. The µ-ring modulator test structures present high-frequency response, and we demonstrated operation up to 25 Gb/s NRZ. The irradiation test results show tolerance to high levels of Total Ionizing Dose (TID) with flawless performance of µ-ring modulators and Ge photodiodes after been irradiated with a TID of 11 MGy.

Why EUROPRACTICE?

The EUROPRACTICE consortium offers a unique opportunity to European universities and research institutes to join multi-project wafer runs and access cutting edge fabrication processes. This is the second PIC that our team manufactures using the imec Silicon Photonics technology. We acknowledge a solid support provided through the EUROPRACTICE framework by imec and Synopsys throughout all phase of the design and testing.

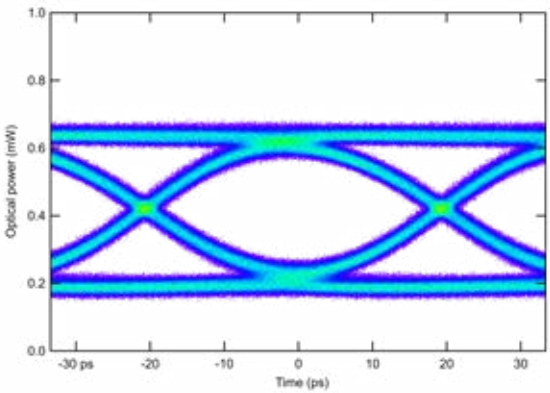

Fig.2: Measured optical eye diagram at 25 Gb/s of one of the ring modulators integrated onto the PIC.

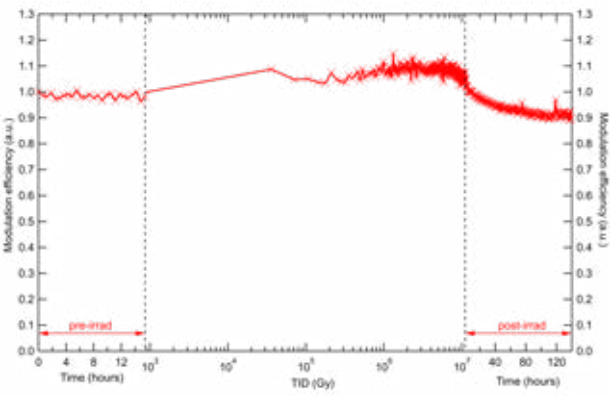

Fig.3: Normalised ring modulator modulation efficiency vs Total Ionising Dose. The device shows flawless performance up to the tested TID of 11 MGy.

DESIGN CONTEST WINNERS

Platform Independent Optimized Rings

Colorado State University, USA

Contacts:	Asif Anwar Baig Mirza, Dr. Mahdi Nikdast
E-mails:	Mirza.Baig@colostate.edu, Mahdi.Nikdast@colostate.edu
Technology:	SiN-Photonics BioPIX300
Die size:	5.3mm x 4.8mm
Application Area:	Education

Introduction

We propose to test the robustness of adiabatic microrings resonators (MRRs) designed in SiN platform. The MRRs have different bus waveguide width and ring waveguide width to improve on robustness. Earlier in our project, we have designed and fabricated MRRs in SiO2 technology and with this run would like to test that our theory is valid regardless of the platform the MRRs are fabricated on. Our team at Colorado State University has been working on a tool that takes into consideration the performance parameters (Q-factor, bandwidth, etc.) from the designer and suggests MRR dimensions (e.g., bus waveguide width, ring waveguide width, thickness, radius, gap) that are helpful to the designer. By proving that adiabatic ring designs are also applicable in the SiN platform we plan to further extend our tool to also include the platform where the chips can be fabricated.

Description

We have used Lumerical FDTD (now Ansys) tools to perform device level simulation. In one of our previous works, we have explored the design space of MRR with Si-SiO2 technology by studying the trends in changes in resonant wavelength due to impact of width and thickness changes in MRR. In such a study, we carefully understood and studied the impact of change of each parameter in MRR (for example radius, gap, width, thickness, etc.). We plan to perform the same set of simulations on a different platform to prove that the same methodology used to design MRRs in Si-SiO2 can also be used for designing MRRs in SiN platform.

The proposed designs haven't been discussed in the SiN platform. There have been mentions of such adiabatic rings in SiO2 platform they have performed well in terms of robustness and improved Q-factor. We would want to verify the same results exist in SiN platform. Extending the research to SiN

platform we should be able to mention that the design space exploration method we propose is independent of SiO2 platform and designers can optimize based on the requirement. By these results, we hope that we would have a much better understanding of the complex microring resonator (MRR) design space.

Studying the pact and robustness of such devices we can extend our study to understand the savings due to such robust designs at not just the device level but at the system and architecture level. This project can pave the way to use more of imec's MPW services for our future designs.

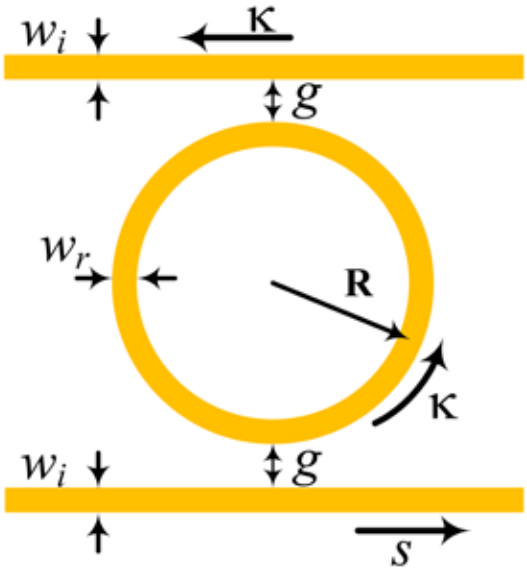

Fig.1: Design of microring resonator (MRR) with input waveguide (wi), ring waveguide (wr), radius (R), and gap (g) showing cross-over coupling (κ) and straight-through coupling (s).

Results

We do not yet have any measurement results but we aim to provide an effective way of addressing the problem of uncertainty in fabrication. In our earlier work we have proved that having different ring waveguide width i.e. different input waveguide width and different coupling waveguide width can help us improve tolerance in microring resonators against fabrication process variations in Si- SiO2 technology. We would want to prove the same point using a different technology (SiN) and make a statement that such a device level optimization is platform independent hence saving energy in terms of compensating for variations at device level. For simulations results we ran a few FDTD simulations using Ansys Lumerical software. We first calculated the impact of width variations on such a material, we look at resonant wavelength shift slope which determines the impact of resonant wavelength shift in a MRR when the waveguide undergoes width variations. We can clearly see that as we increase the waveguide width, the impact of width variations reduces which can be used to our advantage. Another important factor in MRR is the cross-over coupling (κ) when the input and ring waveguide widths (shown in Figure 1) are the same cross-over coupling reduces, however, as we increase the ring waveguide width by keeping the input waveguide constant, we can observe that there is increase in cross-over coupling.

Why EUROPRACTICE?

EUROPRACTICE services has given the fuel necessary to such an idea. Being a university student with limited options to test our theory, EUROPRACTICE has highly appreciated our approach towards proving that device optimization can be done at any given platform.

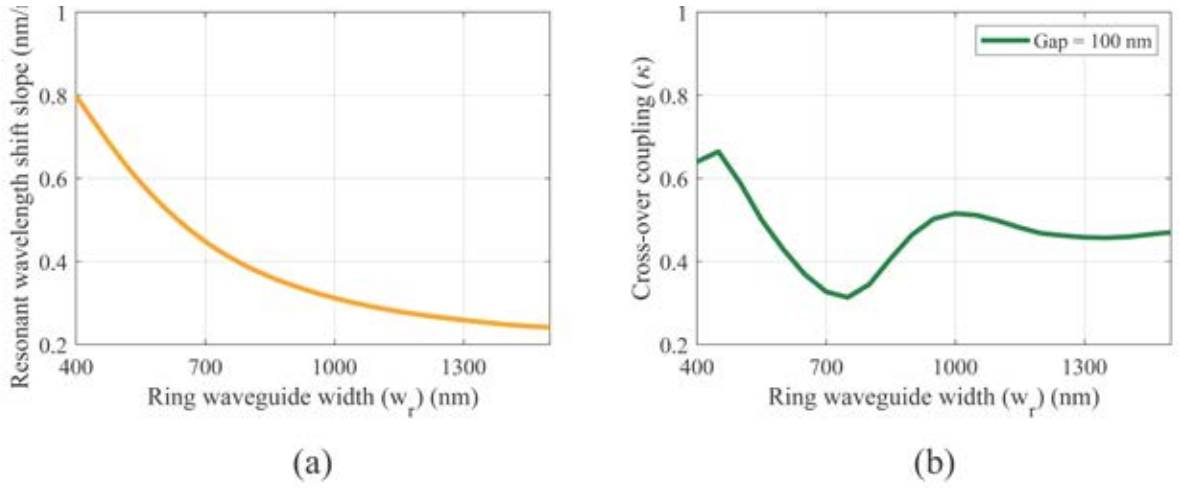

Fig.2: (a) Resonant wavelength shift slope with respect to changes in waveguide width and (b) cross-over coupling (κ) when the input waveguide width is set to 400 nm with a radius of 10 µm and gap of 100 nm.

HVGaNCon – A Flexible Monolithically Integrated Dual Half-Bridge Converter in a High Voltage GaN-on-SOI Technology

The Chair of Integrated Analog Circuits and RF Systems – RWTH Aachen University, Germany

Contacts:	Jan Grobe, Leon Weihs, Michael Hanhart, Ralf Wunderlich, Stefan Heinen
E-mail:	mailbox@ias.rwth-aachen.de
Technology:	imec GaN-IC 650V
Die size:	5180µm x 5180µm
Design Tools:	Cadence Virtuoso, Spectre; Siemens Calibre DRC, PEX, LVS
Application Area:	Research on integrated power electronics

Introduction

The development of switching converters is advancing quickly and has been pushing the performance limits of silicon-based power devices. The development of wide band-gap devices based on Gallium Nitride has opened new possibilities in terms of switching speed and efficiency. Discrete GaN devices have enabled smaller and more efficient designs. However, due to the fast switching-speeds utilized, parasitic inductances are quickly becoming limiting factors. While packaging of single transistors is highly optimized, performance is still limited by the device interconnections. Monolithic integration of switching devices thus allows to further exploit the capabilities of GaN power semiconductors. At the Institute of Integrated Circuits and RF Systems at RWTH Aachen University an integrated power converter was designed in imec's GaN-on-SOI technology to investigate these capabilities and discover their limitations.

Description

The designed integrated circuit is based on a 650 V half-bridge power-stage, which can be employed in various switching converter topologies. The design features integrated gate drivers, optimizing switching time, propagation delay, reducing the impact of external influences and further increasing integration. To enable standalone operation in a buck-configuration, a constant-on-time controller was integrated, consisting of a comparator and analog timing circuitry. The high-side switching signals are translated by a level-shifter, which is designed to operate at switch node slew rates above 500 V/ns. To enable flexible operation, the circuit is reconfigurable ranging from internal regulation to single control of each power transistor.

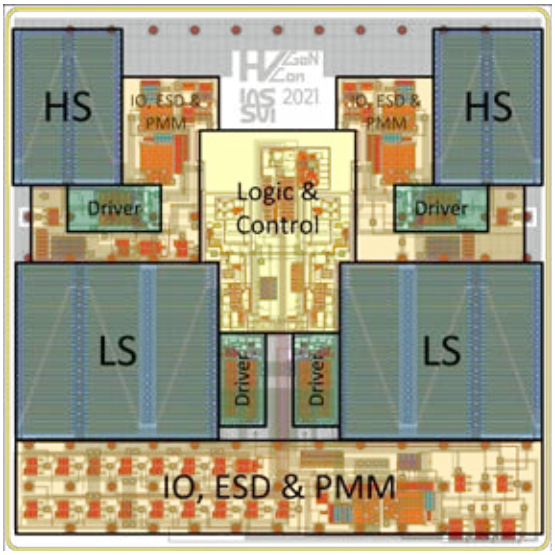

Fig.2: Layout view of the GaN-IC.

Results

The circuit is designed to operate from a wide input voltage range up to 400 V, a nominal output current of 2 A and a switching frequency of up to 5 MHz. The simulation presented in Figure 1 shows a transistor-level simulation of the complete IC starting up for operation as a single-stage 400 V to 48 V buck converter with an input-voltage-step of 40 V and a load-step of 0.5 A. The simulation shows good tracking of the ramped reference voltage, line and load regulation using internal constant on-time control. The layout is presented in Figure 2, with the power-stage, control and miscellaneous subsystems highlighted.

The designed IC will provide insight and further research in converters for operation in high voltage and high frequency automotive applications, as well as off-line converters in consumer applications.

Why EUROPRACTICE?

The Institute of Integrated Circuits and RF Systems has benefited from EUROPRACTICE services in many ways. The access to EDA tools, support and the possibility of participating in various MPW runs including novel technologies such as the one used for this design services offers a great opportunity for universities and research institutions.

Acknowledgements

We would like to express our gratitude towards imec's GaN MPW service for providing a platform for prototyping in a state-of-the-art technology, their support and sponsoring of this tapeout.

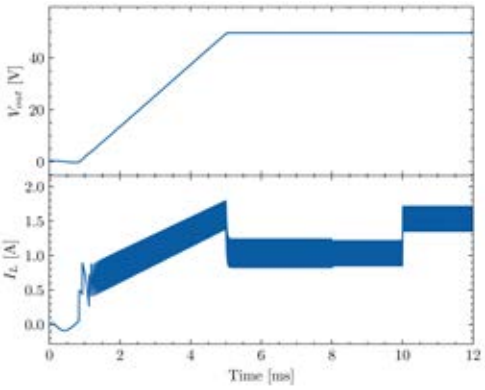

Fig.1: Simulation result of the converter startup and operation.

400V, 1MHz, 200W high-efficiency totem-pole PFC converter

Leibniz University, Hannover, Germany

Contacts:	Niklas Deneke, Tim Rambousky
E-mail:	niklas.deneke@ims.uni-hannover.de
Technology:	imec GaN-IC 650V
Die size:	2.5mm x 5.18mm
Design Tools:	Cadence
Application Area:	Energy

Introduction

The target application field is offline power conversion, i.e., bridgeless power factor correction (PFC) for home appliances and lighting in the 200W power range, which accounts for 60% of the EU residential power consumption [1]. Enhancing the conversion efficiency in this area contributes significantly to reducing global power consumption and related greenhouse gas emission. High switching frequencies supported by GaN enable small passives and more compact solutions while saving valuable resources.

Description

The design includes a fully integrated 650V GaN half-bridge power stage applicable for totem-pole PFC. The IC comprises high-voltage power transistors, gate drivers with short propagation delay, a fast and power-loss optimized level shifter with >200V/ns CMTI suitable for 400V operation and a supply regulator for self-biased offline operation based on previous design experience of the research group [2][3]. The target power level of the demonstrator is at 200W with a power efficiency greater than 99%. Without the availability of low-forward-voltage diodes and complementary devices, innovative protection and clamping circuits are designed to ensure safe operation during switching transitions with slew rates as high as 200V/ns.
Results will be available after fab-out, which is expected by mid-2022.

Why EUROPRACTICE?

EUROPRACTICE enables unique access to imec's 650V GaN-on-SOI technology and provides timely support in this new technology.

Acknowledgements

Thanks to imec's GaN-IC MPW team, especially to Maritza T. Ortiz, for supporting on a variety of aspects during the design phase of the IC.

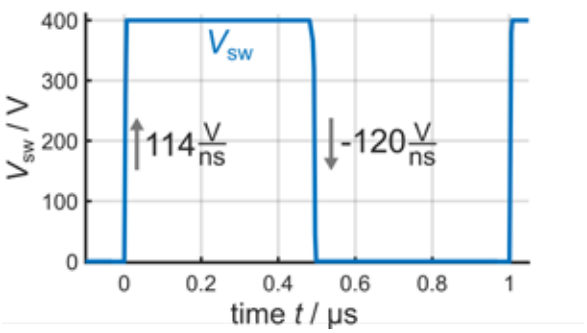

Fig.1: Simulated GaN half-bridge switching behavior (switching output node Vsw).

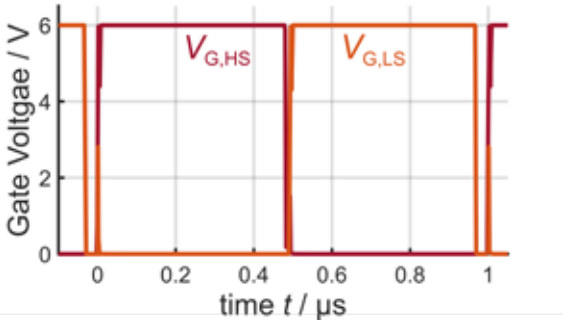

Fig.2: High-side and low-side power HEMT gate voltages VG,HS and VG,LS referenced to the respective ground.

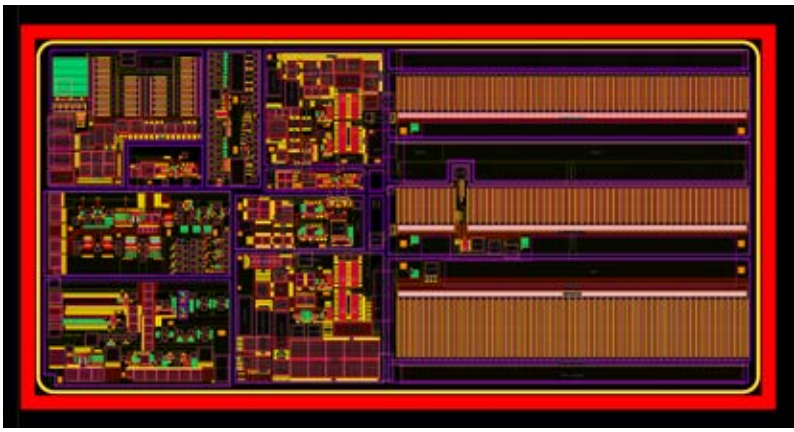

Fig.3: Layout of the 400V, 1MHz PFC GaN converter.

References

[1] https://ec.europa.eu/eurostat/statistics-explained/index.php?title=Energy_consumption_in_households

[2] M. Kaufmann and B. Wicht: A Monolithic GaN-IC with Integrated Control Loop for 400V Offline Buck Operation Achieving 95.6% Peak Efficiency. In IEEE Journal of Solid-State Circuits, vol. 55, pp. 3169 - 3178, December 2020

[3] M. Kaufmann, M. Lueders, C. Kaya, B. Wicht: A Monolithic E-Mode GaN 15W 400V Offline Self-Supplied Hysteretic Buck Converter with 95.6% Efficiency. 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 288-290

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2. **MPW-only annual membership: 600€**
   Allowing full access to all offered MPW runs at discounted pricing.
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   Allowing full access to all the offered CAD tools only.
4. **FPGA-only annual membership: 200€**
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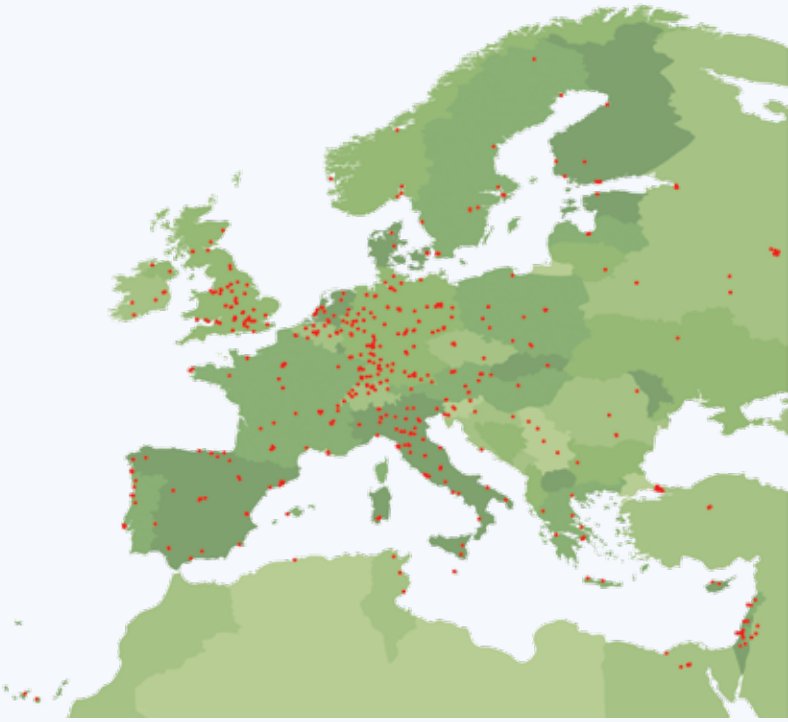
The number of academic members consists of more than 600 institutes in more than 40 countries from the EMEA zone (Europe, Middle East and Africa).



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A38430	Johannes Kepler Universität Linz
R21070	AIT Austrian Institute of Technology
R21210	Österreichische Akademie der Wissenschaften - Wien
R21590	Österreichische Akademie der Wissenschaften - Graz
R22510	Silicon Austria Labs GmbH (Villach)
R22520	Silicon Austria Labs GmbH (Linz)
	Belarus
A47550	Belarusian State University
	Belgium
A13940	Université de Liège
A35651	Université Catholique de Louvain
A35880	Universiteit Gent
A37190	Universiteit Antwerpen
A37210	Vrije Universiteit Brussel
A37220	Katholieke Universiteit Leuven
A38160	Université de Mons
A38190	Université Libre de Bruxelles
R00040	imec
R21440	Studiecentrum voor Kernenergie - Centre d'Etude de l'énergie Nucléaire

Bosnia and Herzegovina

A48180	Univerzitet u Banjoj Luci

Bulgaria

A40090	Technical University of Sofia

Croatia

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A47920	Sveuciliste J.J. Strossmayera
A48090	Sveuciliste u Splitu

Cyprus

A07090	University of Cyprus

Czech Republic

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A40070	Vysoke uceni technicke v Brne
R22660	Institute of Organic Chemistry and Biochemistry
R47460	Akademie ved Ceske republiky
R49000	Ustav teorie informace a automatizace AV CR

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A15090	The German University in Cairo
A15160	The American University in Cairo
A15170	Egypt-Japan University of Science & Technology
A16020	Zewail City of Science & Technology
R22620	Electronics Research Institute

Estonia

A40110	Tallinna Tehnikaülikool

Finland

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A35040	Aalto-yliopisto
A35610	Tampereen teknillinen yliopisto
A35820	Oulun yliopisto
A39360	Turun yliopisto
R14360	Fysiikan tutkimuslaitos
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A37470	Université de Strasbourg
A37590	Aix Marseille Université
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A37980	Université Joseph Fourier
A39060	Laboratoire d'Annecy-le-Vieux de physique des particules
A39400	Université Clermont Auvergne
R00210	Laboratoire d'Analyse et d'Architectures des Systèmes
R14140	Laboratoire des sciences de l'ingénieur, de l'informatique et de l'imagerie
R15140	XLIM Université de Limoges
R20490	European Synchrotron Radiation Facility
R20810	Station de Radioastronomie de Nançay, Observatoire de Paris
R20980	Laboratoire des Plasmas et de Conversion d'Energie
R21020	Synchrotron SOLEIL
R21030	Institut Matériaux Microélectronique Nanosciences de Provence
R21140	Institut Laue-Langevin
R21170	Laboratoire de l'Accélérateur Linéaire
R21270	Commissariat à l'énergie atomique et aux énergies alternatives - IRFU
R21290	Spintronique et Technologie des Composants
R21380	Laboratoire de Physique des Plasmas
R21560	Office National d'Études et de Recherches Aérospatiales - Toulouse
R21960	Institut de recherche en astrophysique et planétologie
R22060	Institut d'Astrophysique Spatiale
R22210	Centre de Microélectronique OMEGA
R22240	Le Laboratoire Procédés, Matériaux et Énergie Solaire
R22280	Institut de Recherche sur les Composants logiciels et matériels pour l'Information et la Communication Avancée
R22310	Grand Accélérateur National d'Ions Lourds
R22360	Institut de Recherche et Technologie Antoine de Saint Exupéry
R22590	Circuits Multi-Projets
R22680	Institut des Sciences Chimiques de Rennes
R22730	CEA Saclay IRAMIS
R22780	Centre d'Élaboration de Matériaux et d'Etudes Structurales
R37850	Laboratoire de Physique des 2 Infinis Irène Joliot-Curie
R38290	Laboratoire de l'Intégration du Matérieu au Système

Germany

A00110	Johannes Gutenberg Universität Mainz
A00240	Fachhochschule Köln
A00510	Hochschule Konstanz für Technik, Wirtschaft und Gestaltung
A00670	Hochschule Bremen
A00850	Justus Liebig-Universität Gießen
A12140	Technische Universität München - Fakultät für Physik (Garching)
A12270	Hochschule Albstadt-Sigmaringen
A12410	Fachhochschule Schmalkalden
A12440	Hochschule Pforzheim
A12540	Brandenburgische Technische Universität Cottbus
A12840	Bergische Universität Wuppertal
A13060	Albert-Ludwigs-Universität Freiburg - IMTEK
A13610	Fachhochschule Aachen
A13660	Universität Bremen - Informatik
A13680	Technische Hochschule Aschaffenburg
A13890	Technische Universität Berlin - Institut für Technische Informatik und Mikroelektronik (TIME)
A14130	Fachhochschule Brandenburg
A14310	Universität Kassel - Fachbereich Elektrotechnik/Informatik
A14740	Universität Kassel
A15030	Universität Bielefeld
A15230	Hochschule für Angewandte Wissenschaften Hamburg
A15410	Technische Hochschule Mittelhessen - Friedberg
A15500	Hochschule RheinMain
A15840	Hochschule Rosenheim
A15930	Fachhochschule Südwestfalen
A15950	Beuth Hochschule für Technik Berlin
A16030	Rheinisch-Westfälische Technische Hochschule Aachen - Lehrstuhl für Integrierte Photonik (IPH)
A16040	Rheinisch-Westfälische Technische Hochschule Aachen - Institut für Stromrichtertechnik und Elektrische Antriebe (ISEA)

A16060	Rheinisch-Westfälische Technische Hochschule Aachen - Institut für Theoretische Elektrotechnik (ITHE)
A16090	Westfälische Hochschule
A16100	Hochschule fuer Technik und Wirtschaft Berlin (HTW Berlin)
A16310	Technische Universität Bergakademie Freiberg
A16320	RWTH Aachen, Physikalisches Institut B
A16330	Hochschule Hannover
A16450	Universität Mannheim
A16490	Universität Bayreuth
A16520	Westfälische Wilhelms-Universität
A16590	IUBH University of Applied Sciences
A16610	University of Bremen / BCCMS
A16640	University of Applied Science Nordhausen
A16650	University of Passau
A16680	Technische Hochschule Lübeck
A35320	Technische Universität Hamburg-Harburg
A35400	Hochschule Ulm
A35420	Georg-Simon-Ohm Hochschule Nürnberg
A35430	Karlsruher Institut für Technologie
A35450	Technische Universität Darmstadt - Integrierte Elektronische Systeme (IES)
A35500	Eberhard Karls Universität Tübingen
A35590	Johannes-Wolfgang-Goethe-Universität Frankfurt am Main
A35600	Technische Universität Carolo-Wilhelmina zu Braunschweig
A35620	Universität Bremen - Institut für Theoretische Elektrotechnik und Mikroelektronik
A35710	Hochschule Augsburg
A35810	Technische Universität Kaiserslautern
A35830	Universität Hamburg
A35990	Universität Duisburg-Essen
A36070	Carl von Ossietzky Universität Oldenburg - Informatik
A36440	Universität des Saarlandes
A37090	Technische Universität Dortmund
A37240	Hochschule Furtwangen
A37290	Leibniz Universität Hannover
A37310	Technische Universität Berlin
A37380	Friedrich-Alexander-Universität Erlangen-Nürnberg
A37390	Technische Universität München - Fakultät für Elektrotechnik und Informationstechnik München
A37440	Universität der Bundeswehr München
A37450	Hochschule Esslingen
A37500	Universität Paderborn
A37510	Hochschule für Angewandte Wissenschaften München
A37530	Humboldt-Universität zu Berlin
A37540	Universität Ulm
A37760	Technische Universität Dresden
A37800	Hochschule Offenburg
A37810	Rheinisch-Westfälische Technische Hochschule Aachen - Fakultät für Elektrotechnik und Informationstechnik
A37880	Hochschule Aalen
A37920	Hochschule Ravensburg-Weingarten
A37930	Hochschule Mannheim
A38010	Hochschule Heilbronn
A38030	Hochschule Darmstadt
A38080	Ruhr-Universität Bochum
A38090	Otto-von-Guericke-Universität Magdeburg
A38220	Universität Siegen
A38240	Technische Universität Ilmenau
A38340	Technische Universität Chemnitz
A38550	Ostfalia Hochschule für angewandte Wissenschaften
A38650	Fachhochschule Dortmund
A38890	Rheinische Friedrich-Wilhelms-Universität Bonn
A38940	Ernst-Abbe-Fachhochschule Jena
A39000	Technische Hochschule Mittelhessen - Gießen
A39070	Hochschule Karlsruhe - University of Applied Sciences
A39110	Universität Stuttgart
A39220	Universität Rostock
A39250	Ruprecht-Karls-Universität Heidelberg - ASIC
A39260	Albert-Ludwigs-Universität Freiburg
A39330	Hochschule Reutlingen
A39340	Martin-Luther-Universität Halle-Wittenberg
A39460	Christian-Albrechts-Universität zu Kiel
A39580	Hochschule Osnabrück
A39660	Friedrich-Schiller-Universität Jena
A39770	Universität zu Lübeck
R00150	Max-Planck-Institut für Physik
R20300	Institut für Mikroelektronik- und Mechatronik - Systeme gemeinnützige GmbH
R20330	Deutsches Elektronen-Synchrotron
R20460	Institut für Mobil- und Satellitenfunktechnik GmbH
R20510	IHP GmbH - Leibniz-Institut für innovative Mikroelektronik
R20570	Fraunhofer-Institut für Techno- und Wirtschaftsmathematik
R20720	Oldenburger Forschungs- und Entwicklungsinstitut für Informatik-Werkzeuge und -Systeme
R20880	GSI Helmholtzzentrum für Schwerionenforschung GmbH
R20890	Fraunhofer-Institut für Siliziumtechnologie
R20920	Fraunhofer-Institut für Integrierte Schaltungen - Erlangen
R20930	Fraunhofer-Institut für Integrierte Schaltungen - Dreden
R21050	Max-Planck-Institut für Chemie
R21060	Forschungszentrum Jülich
R21090	Fraunhofer Heinrich-Hertz-Institut
R21120	Max-Planck-Institut für extraterrestrische Physik
R21150	Physikalisch-Technische Bundesanstalt - Braunschweig
R21220	Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie
R21260	Hochschule für Technik und Wirtschaft Dresden
R21310	Fraunhofer-Institut für Photonische Mikrosysteme
R21320	Fraunhofer-Institut für Solare Energiesysteme
R21510	Deutsches Zentrum für Luft- und Raumfahrt - Berlin
R21530	Deutsches Zentrum für Luft- und Raumfahrt - Bremen
R21580	Deutsches Zentrum für Luft- und Raumfahrt IIP - Berlin
R21610	Helmholtz-Zentrum Berlin für Materialien und Energie
R21620	Fraunhofer-Einrichtung für Angewandte und Integrierte Sicherheit
R21630	Fraunhofer-Institut für Zerstörungsfreie Prüfverfahren
R21650	Fraunhofer-Institut für Hochfrequenzphysik und Radartechnik
R21660	Fraunhofer-Einrichtung für Systeme der Kommunikationstechnik
R21770	Konrad-Zuse-Zentrum für Informationstechnik Berlin
R21780	Deutsches Zentrum für Luft- und Raumfahrt - Wessling
R21790	NaMLab gGmbH
R21900	Max-Planck-Institut für Radioastronomie
R21970	PNSensor gGmbH
R22020	European XFEL
R22080	Fraunhofer Institute for Organic Electronics, Electron Beam and Plasma Technology FEP
R22110	Physikalisch-Technische Bundesanstalt - Berlin
R22150	Fraunhofer Institute SIT
R22160	Halbleiterlabor der Max Planck Gesellschaft
R22260	Helmholtz-Zentrum Geesthact
R22290	Fraunhofer-Einrichtung für Mikrosysteme und Festkörper-Technologien EMFT
R22370	CIS Forschungsinstitut fuer Mikrosensorik GmbH
R22440	Hahn-Schickard-Gesellschaft fuer Angewandte Forschung e.V.
R22500	Max-Planck-Institut für Mikrostrukturphysik
R22530	European Molecular Biology Laboratory
R22650	Max-Planck-Institute for Software Systems
R22670	Institut für Mikroelektronik Stuttgart
R22690	Max-Planck-Institut für Quantenoptik
R22710	Fraunhofer Institut fuer Mikroelektronische Shaltungen und Systeme (IMS)
R22770	CISPA-Helmholtz-Zentrum Fur Informaitonssicherheit gGmbH

Ghana

A14770	Kwame Nkrumah University of Science & Technology

Greece

A00530	University of Ioannina
A13550	University of Thessaly
A14150	Athens University of Economics and Business
A14700	University of Piraeus
A16630	University of West Attica
A16720	National and Kapodistrian University of Athens
A35140	National Technical University of Athens
A35960	University of Patras - Electrical and Computer Engineering
A37550	National and Kapodistrian University of Athens
A37680	University of Patras
A39280	Aristotle University of Thessaloniki
A39490	Technical University of Crete
R20790	Demokritos, National Center for Scientific Research
R21080	Foundation for Research and Technology Hellas
R22640	Athena Research Centre

Hungary

A40010	Budapesti Muszaki és Gazdaságtudományi Egyetem
A47540	Pázmány Péter Katolikus Egyetem

Ireland

A01190	Munster Technological University
A13410	Institute of Technology, Carlow
A15730	University College Dublin
A35300	University College Cork
A36510	University of Limerick
A39310	Technological University Dublin, Tallaght Campus
R21720	Tyndall National Institute
R22400	Dublin Institute for Advanced Studies

Israel

A13240	The Hebrew University of Jerusalem
A13330	Technion - Israel Institute of Technology
A13910	Ben-Gurion University of the Negev
A13920	Bar-Ilan University
A14070	Ort Braude College of Engineering
A14380	Tel-Aviv University
A14540	Kinneret College on the Sea of Galilee
A14690	Holon Institute of Technology
A15190	Jerusalem College of Technology
A16530	The Academic College of Tel Aviv Yaffo

Italy

A00120	Università Politecnica delle Marche
A00520	Università degli Studi di Modena e Reggio Emilia - Modena
A00560	Università degli Studi di Siena
A00680	Università della Calabria
A00740	Università degli Studi di Perugia
A12000	Università di Bologna - DEIS
A12370	Università degli Studi di Napoli Federico II - DIETI
A12390	Università degli Studi di Brescia
A12530	Università degli Studi di Verona
A12640	Università degli Studi di Milano
A12770	Università del Salento
A12990	Università degli Studi di Bergamo
A13280	Università degli Studi di Udine
A14220	Università degli Studi di Trento
A14800	Università degli Studi di Milano-Bicocca
A14820	Università degli Studi di Salerno
A14860	Università degli Studi di Modena e Reggio Emilia - Reggio Emilia
A15070	Scuola Superiore di Studi Universitari e di Perfezionamento Sant'Anna
A15750	Università Degli Studi di Cassino e del Lazio Meridionale
A15900	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Cesena)
A16130	Università degli Studi Roma Tre
A16460	Politecnico di Bari
A16570	University of Bologna
A35210	Università degli Studi di Parma
A35530	Politecnico di Torino
A35660	Università di Pisa
A35690	Politecnico di Milano
A35910	Università degli Studi di Genova
A36380	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Bologna)
A37280	Università degli Studi di Pavia
A37460	Università degli Studi di Catania
A38380	Politecnico di Bari
A38620	Università degli Studi di Torino
A38840	Università degli Studi di Roma "La Sapienza"
A39200	Università degli Studi di Padova
A39410	Università degli Studi dell'Aquila
A39550	Università degli Studi di Firenze
A39570	Università degli Studi di Cagliari
R00140	Fondazione Bruno Kessler
R00270	Istituto Nazionale di Fisica Nucleare, Sezione di Genova
R00300	Istituto Nazionale di Fisica Nucleare, Sezione di Pisa
R20310	Istituto Nazionale di Fisica Nucleare, Sezione di Roma
R20320	Istituto Nazionale di Fisica Nucleare, Sezione di Roma II
R20400	Istituto Nazionale di Fisica Nucleare, Sezione di Bologna
R20420	Istituto Nazionale di Fisica Nucleare, Sezione di Trieste
R20440	Istituto Nazionale di Fisica Nucleare, Sezione di Torino
R20450	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali di Frascati
R20470	Istituto Nazionale di Fisica Nucleare, Sezione di Padova
R20550	Elettra-Sincrotrone Trieste
R20630	Istituto Nazionale di Fisica Nucleare, Sezione di Milano
R20670	Istituto Nazionale di Fisica Nucleare, Sezione di Cagliari
R20710	Istituto Nazionale di Fisica Nucleare, Sezione di Bari
R20990	Istituto Nazionale di Fisica Nucleare, Sezione di Ferrara
R21100	Istituto Nazionale di Fisica Nucleare, Sezione di Napoli
R21160	Istituto Nazionale di Astrofisica, Osservatorio Astrofisico di Arcetri
R21190	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali del Gran Sasso
R21300	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi
R21450	Istituto Nazionale di Fisica Nucleare, Sezione di Pavia
R21570	Istituto Nazionale di Astrofisica, Istituto di Radioastronomia
R21600	Istituto Italiano di Technologia
R21800	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi Roma
R21940	The Abdus Salam International Centre for Theoretical Physics
R22010	Istituto Nazionale di Astrofisica Osservatorio Astronomico di Cagliari
R22070	Instituto per lo Studio dei Materiali Nanostrutturati
R22120	Istituto Nazionale di Astrofisica - Istituto di Radioastronomia - Radiotelescopi di Medicina
R22200	Radio Analog Micro Electronics srl
R22390	Instituto Nazionale di Fisica Nucleare Sezione di Perugia
R22450	European Gravitational Observatory
R22490	Istituto Nazionale di Fisica Nucleare
R22550	Consorzio Nazionale Interuniversitario per le Telecomunicazioni
R22790	Instituto Nanoscienze - CNR
R22490	Istituto Nazionale di Fisica Nucleare
R22550	Consorzio Nazionale Interuniversitario per le Telecomunicazioni

Jordan

A15990	Princess Sumaya University for Technology
A16470	German Jordanian University

Kazakhstan

A48080	Nazarbayev University

Latvia

A48060	Riga Technical University
R49020	Institute of Electronics & Computer Science

Lebanon

A15720	Lebanese American University
A47650	American University of Beirut
R22630	Houmal Technology Park

Lithuania

A47980	Vilniaus Universitetas
R49200	Baltic Institute of Advanced Technology (BPTI)

Malta

A38720	University of Malta

Norway

A12750	Høgskolen i Sørøst-Norge
A37360	Universitetet i Oslo
A37560	Norges Teknisk Naturvitenskapelige Universitet - Institutt for elektroniske systemer
A37820	Universitetet i Bergen
R21460	SINTEF Stiftelsen for industriell og teknisk forskning

Palestine

A16240	Birzeit University
A16370	An-Najah National University

Poland

A40100	Uniwersytet Zielonogórski
A40120	Politechnika Warszawska
A40130	Politechnika Lódzka - Mikroelektroniki I Technik Informatycznych (DMCS)
A40140	Akademia Górniczo-Hutnicza im. Stanislawa Staszica
A40150	Instytut Fizyki Jadrowej im. Henryka Niewodniczanskiego
A40160	Politechnika Wroclawska
A40530	Politechnika Slaska
A47300	Politechnika Gdanska
A47400	Politechnika Poznanska - Inzynierii Komputerowej
A47670	Politechnika Poznanska - Radiokomunikacji
A47740	Politechnika Lódzka - Pólprzewodnikowych I Optoelektronicznych
R22610	Institute of High Pressure Physics (UNIPRESS)
R40030	Siec Badawcza Lukasiewicz - Instytut Mikroelektroniki I Fotoniki
R49030	Instytut Podstawowych Problemów Techniki PAN (IPPT-PAN)
R49080	Centrum Badan Kosmicznych PAN

Portugal

A12310	Universidade Nova de Lisboa
A12550	Universidade do Minho
A13710	Instituto Superior de Engenharia de Lisboa
A35540	Universidade do Porto
A35670	Universidade de Aveiro
A35970	Instituto Superior Técnico
A37230	Instituto de Engenharia de Sistemas e Computadores - Investigação e Desenvolvimento
R14120	Instituto de Telecomunicações - Lisboa
R21710	Laboratório de Instrumentação e Física Experimental de Partículas
R21750	International Iberian Nanotechnology Laboratory
R21890	Instituto de Telecomunicações - Aveiro
R22170	Instituto de Sistemas Robótica (ISR-UC)

Romania

A15520	Universitatea Politehnica din Bucuresti
A15560	Universitatea Tehnică "Gheorghe Asachi" din Iaşi
A16070	Universitatea Transilvania Brasov
A47880	Universitatea Politehnica din Timişoara
A48070	Universitatea Tehnica din Cluj-Napoca
R49010	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Nuclear Hadrons
R49060	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Particle Physics

Russia

A40240	Vladimir State Technical University named after Alexander and Nikolay Stoletovs
A47330	St. Petersburg State Polytechnical University
A47520	National Research University of Electronic Technology (MIET)
A47790	St. Petersburg State University of Aerospace Instrumentation
A47810	Lomonosov Moscow State University
A47850	Moscow Institute of Physics & Technology (MIPT) - Wireless Technologies
A47990	St. Petersburg Electrotechnical University 'LETI'
A48030	Omsk State Technical University
A48040	Moscow Institute of Physics & Technology (MIPT) - Control Systems
A48130	Ufa State Aviation Technical University
A48140	Ulyanovsk State University
A48160	Southern Federal University
A60030	Tomsk State University
A60040	Tomsk State University of Control Systems and Radioelectronics
A60060	Mordovian State University named after N.P.Ogarev
A60080	Novosibirsk State Technical University
A60100	National Research University Higher School of Economics
A60110	National Research Nuclear University MEPHI
A60150	Moscow Institute of Physics & Technology (MIPT) - Photonics
A60160	Bauman Moscow State Technical University - Kaluga
A60170	Moscow State Technical University of Radioengineering, Electronics and Automation
A60190	Bauman Moscow State Technical University - Moscow
A60200	ISP, Novosibirsk State University
A60220	Voronezh State Academy of Forestry Engineering
A60230	Samara National Research University (Samara University)
A60240	National University of Science & Technology 'MISiS'
A60250	Bryansk State Technical University
R21930	Scientific Manufacturing Complex "Technological Centre" MIET (SMCTC)
R47900	Budker Institute of Nuclear Physics
R49070	Space Research Institute (IKI)
R49210	Institute of Physical Materials Science (IPMS SB RAS)
R49220	Institute of Nanotechnology of Microelectronics of the Russian Academy of Sciences

Serbia

A47510	Univerzitet u Nišu
A47600	Univerzitet u Novom Sadu
A48010	Univerzitet u Beogradu
A48170	Univerzitet u Kragujevcu
A48200	Univerzitet u Novom Sadu
R49230	BioSense Institute

Slovakia

A40050	Slovenská technická univerzita v Bratislave
A47930	Technická univerzita v Kosiciach

Slovenia

A40280	Univerza v Ljubljani
A47690	Institut "Jozef Stefan"
A47820	Univerza v Mariboru
R22580	Skylabs Vesoljske Tehnologije Doo

South Africa

A14560	University of Pretoria

Spain

A12320	Universidad Politécnica de Cartagena
A12590	Universidad de Castilla - La Mancha
A13150	Universitat de València
A13340	Universidad de Alcalá
A13860	Universidad de Salamanca
A14720	Universidad de La Laguna
A15370	Universidad de Deusto
A16290	Universitat Pompeu Fabra
A16340	University of Vigo - AtlanTTic
A35130	Universidad Politécnica de Madrid - Departamento de Ingeniería Electrónica
A35190	Universitat Politècnica de València
A35870	Universidad de Sevilla - Instituto de Microelectrónica de Sevilla (IMSE-CNM)
A35891	Universidad de Cantabria
A36250	Universitat Autònoma de Barcelona
A36390	Universidad de Las Palmas de Gran Canaria - Instituto Universitario de Microelectrónica Aplicada (IUMA)
A37060	Universidad de Zaragoza - Dpto.Ingenieria Electronica y Comunicaciones
A37080	Universidad de Santiago de Compostela
A37330	Universidad Complutense de Madrid
A37580	Universidad de Malaga
A37690	Universidad del Pais Vasco
A38330	Universidad de Vigo
A38360	Universitat de les Illes Balears
A38580	Universidad de Sevilla - Ingenieria Electronica
A38590	Universidad de Granada
A38600	Universidad de Navarra
A38660	Universitat de Barcelona
A38780	Universidad de Las Palmas de Gran Canaria - Departamento de Informàtica y Sistemas
A38790	Universidad de Zaragoza - Facultad de Ciencias
A38820	Universidad Politécnica de Madrid - Centro de Electrónica Industrial
A39080	Universidad de Extremadura
A39100	Universidad Pública de Navarra
A39150	Universitat Politècnica de Catalunya - Departamento de Ingeniería Electrónica (Campus Nord)
A39180	Universitat Rovira i Virgili
A39390	Universitat Autónoma de Madrid
A39540	Universidad Carlos III de Madrid
R00060	CNM - Instituto de Microelectrónica de Barcelona
R20700	Ikerlan
R20850	Centre Tecnològic de Telecomunicacions de Catalunya
R21230	Instituto de Fisica Corpuscular
R21520	Institute of Space Sciences (ICE-CSIC)
R21550	Institut de Ciències Fotòniques
R21740	Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas
R21910	Instituto de Tecnologías Físicas y de la Información
R22100	Centro Nacional de Supercomputación, Barcelona
R22460	Consorcio ESS Bilbao

Sweden

A00260	Luleå tekniska universitet
A13720	Uppsala universitet
A16350	Stockholms universitet
A16360	Kungliga Tekniska Hogskolan, Stockholm
A16730	Linnéuniversitetet
A37350	Linköpings universitet
A37370	Lunds universitet
A38180	Kungliga Tekniska högskola, Kista
A38670	Chalmers Tekniska högskola
A39840	Mittuniversitetet
R20690	Research Institutes of Sweden, ICT Acreo
R20910	Totalförsvarets forskningsinstitut FOI
R21700	MAX IV Laboratory
R21990	European Spallation Source
R22050	Institutet för Rymdfysik

Switzerland

A05000	Scuola Universitaria Professionale della Svizzera Italiana
A12730	École Polytechnique Fédérale de Lausanne - Laboratoire de Physique des Hautes Energies
A12920	Universität Zürich
A13090	Università della Svizzera Italiana
A13630	Université de Genève
A14780	Haute école d'ingénierie et d'architecture Fribourg
A15480	Universität Basel
A15530	Universität Bern
A16440	Universität Zurich
A36110	École Polytechnique Fédérale de Lausanne - Microelectronics Systems
A37340	École Polytechnique Fédérale de Lausanne - Neuchâtel
A38100	Ostschweizer Fachhochschule
A38310	Eidgenössische Technische Hochschule Zürich
A38410	Berner Fachhochschule
A38800	Eidgenössische Technische Hochschule Zürich - Basel
A39820	University of Applied Sciences and Arts Northwestern Switzerland
R20350	Organisation Européenne pour la Recherche Nucléaire
R20680	Centre Suisse d'Electronique et Microtechnique - Neuchâtel
R20800	Paul Scherrer Institut
R20970	Centre Suisse d'Electronique et Microtechnique - Zürich
R22180	Eidgenössische Materialprüfungs- und Forschungsanstalt
R20970	Centre Suisse d'Electronique et Microtechnique - Zürich
R22180	Eidgenössische Materialprüfungs- und Forschungsanstalt

The Netherlands

A00170	Universiteit Twente - CAES
A12010	Vrije Universiteit Amsterdam
A12650	Radboud Universiteit Nijmegen
A13730	Stichting Saxion
A14510	Rijksuniversiteit Groningen
A15420	Erasmus Universitair Medisch Centrum Rotterdam
A15960	Universiteit van Amsterdam
A35701	Technische Universiteit Delft
A38050	Technische Universiteit Eindhoven
R00280	Nikhef
R20370	TNO-FEL
R20430	European Space Agency - ESTEC Microelectronics
R20520	Stichting Nederlandse Wetenschappelijk Onderzoek Instituten / Stichting ASTRON, Netherlands Institute for Radio Astronomy
R20540	European Space Agency - ESTEC Payload Technology
R21200	Stichting imec Nederland
R21250	NWO-I/SRON

Tunisia

A12930	École Nationale d'ingénieurs de Sfax
A15300	École Nationale d'ingénieurs de Tunis
R22570	Center for Research in Microelectronics and Nanotechnology

Turkey

A13010	Sabanci Üniversitesi
A13270	Hacettepe Üniversitesi
A13530	TC Kocaeli Üniversitesi
A13820	Koc Universitesi

A14250	Yeditepe Üniversitesi
A14730	TOBB Ekonomi ve Teknoloji Üniversitesi
A15280	Orta Dogu Teknik Üniversitesi Kuzey Kibris Kampusu
A15680	Ankara Yildirim Beyazit Üniversitesi
A15870	Istanbul Bilgi Üniversitesi
A15970	Özyegin Üniversitesi
A16250	Istanbul Medipol Üniversitesi
A16550	Maltepe University
A16660	Atilim University
A37960	Istanbul Teknik Üniversitesi
A38270	Ihsan Dogramaci Bilkent Üniversitesi
A38440	Orta Dogu Teknik Üniversitesi
A39170	Bogaziçi Üniversitesi
R22740	TUBITAK - UME (National Metrology Institute of Turkey)
R38860	Türkiye Bilimsel ve Teknik Arastirma Kurumu -BILGEM

UK

A12480	University of Bath
A13480	Imperial College London
A13510	Royal Holloway University of London
A13520	University College London
A13620	University of Manchester Jodrell Bank Observatory
A14580	University of Lincoln
A14750	UCL Mullard Space Science Laboratory
A14980	Queen Mary University of London
A15390	The Open University
A15450	Cardiff University
A15790	City University London
A16000	Coventry University
A16050	Cranfield University
A16580	University of Chester
A16670	University of Exeter, Penryn Campus
A35030	Sheffield Hallam University
A35080	University of Manchester
A35111	University of Sussex
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A35330	Newcastle University
A35410	University of Hull
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A36280	Brunel University
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A37400	University of Huddersfield
A37420	University of Edinburgh
A37430	University of the West of England
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A37570	University of Surrey
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A37610	University of Southampton
A37630	University of Warwick
A37660	Swansea Metropolitan University
A37730	University of Leeds
A37780	University of South Wales
A37840	University of Durham
A37870	Swansea University
A37900	Manchester Metropolitan University
A38040	Oxford Brookes University
A38450	Loughborough University
A38810	University of York
A39440	University of Glasgow
A39450	Aston University
A39650	University of Salford
R00050	STFC Rutherford Appleton Laboratory
R20600	STFC Daresbury Laboratory
R20950	Diamond Light Source
R22030	STFC UK Astronomy Technology Centre
R22090	Culham Centre for Fusion Energy
R20600	STFC Daresbury Laboratory
R20950	Diamond Light Source
R22030	STFC UK Astronomy Technology Centre
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All information for fabrication support, MPW run schedules and prices is available on our Technology & Fabrication website

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Design tools are available to Academic Institutions and publicly funded Research Laboratories in the EMEA region. More information can be obtained on our Design Tool & Training website

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